Low Voltage, Low Power 4-Bit Microcontroller

The **M44C636** is a member of the **MARC4** family of low cost, single chip CMOS microcontrollers. This 4-bit µC contains an on-chip RC oscillator, CPU core, 4 KByte ROM, 253 x 4-bit RAM, 16 I/O lines, 32-kHz crystal oscillator, 15 stage prescaler with two watch timer interrupts, two independent 8-bit multifunction timer/counters, hardware watchdog timer and liquid crystal display driver circuitry.

Features

- 4 bit stack oriented Harvard architecture
- 4 K x 8-bit application ROM
- 253 x 4-bit of on-chip RAM
- 13 bidirectional I/O lines
- 4 input lines with interrupt and coded reset facility
- 2 × 8-bit multifunction timer/counter
- 3 external, 2 timer/counter and 2 watch timer interrupts
- Programmable LCD driver for up to 80 segments
- Built-in LCD voltage generation with temperature compensation

Benefits

- Dual supply voltage range (1.2 to 2.4 V or 1.8 to 3.6 V with integrated regulator)
- Separate watch crystal oscillator for time keeping
- Power saving and SLEEP mode (< 1 µA)
- Data retention down to 0.9 V in SLEEP mode
- Fully integrated, fast on-chip RC oscillator
  – 2 / 4 µs instruction cycle time at 1.5 / 1.2 V
  – 4 µs from 1.8 to 3.6 V with internal voltage regulator
- Watchdog, master reset input and static power-on reset circuit with ”brown–out” function
- High level programming language qFORTH
- PC based development tools
- Comprehensive library of software routines
- Piggyback version for program evaluation

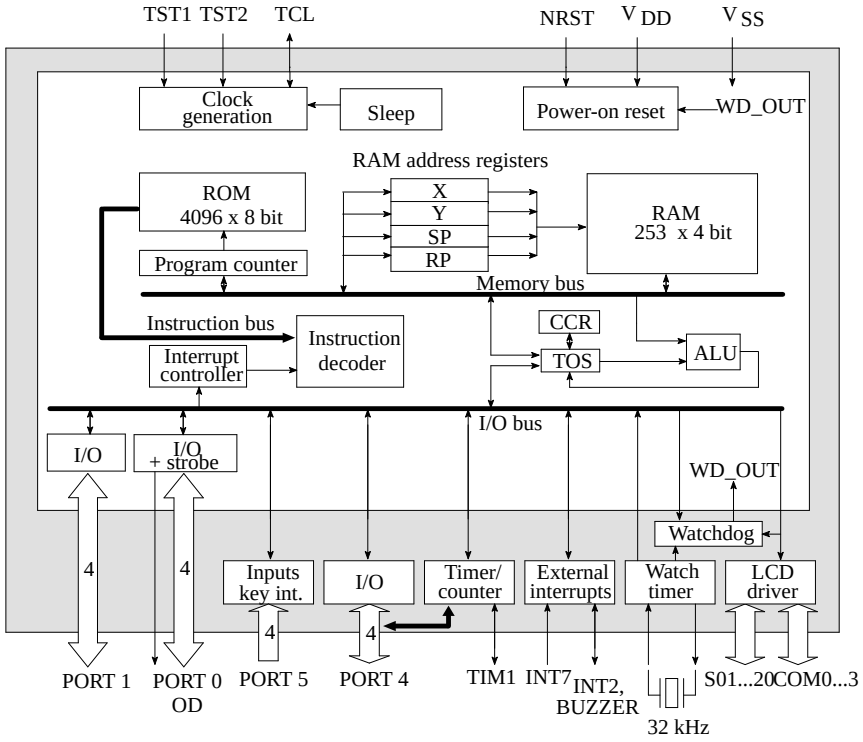

Figure 1. M44C636 – functional block diagram

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Contents (continued)

Contents (continued)

1 Signal Description, I/O Programming, Memory, Core Registers, and Self-Check

1.1 Signal Description

1.1.1 V_{DD}, V_{SS}, AV_{DD} and AV_{SS}

Power is supplied to the microcontroller using these pins. V_{DD} is power for the µC core, RAM, ROM and the peripherals, V_{SS} is ground. AV_{DD} is power for the crystal oscillator and AV_{SS} is ground.

1.1.2 V_{REG}, V_{EE1}, V_{EE2}, C1 and C2

V_{REG} is the temperature compensated reference for the LCD voltage booster circuitry. It is used for building up the doubled (**V_{EE1}**) and tripled (**V_{EE2}**) voltage levels required by multiplexed low voltage LCDs. The pump capacitor for the voltage generator is connected between **C1** and **C2**. Storage capacitors must be attached at **V_{EE1}** and **V_{EE2}** towards V_{SS} (see figure 32). **V_{REG}** is generated internally for 3 V LCD panels.

1.1.3 NRST

The **NRST** input is required for a proper power-on start up but can be used to reset the internal state of the microcontroller and provide an orderly software start-up procedure. The integrated power-on circuitry provides a time delay from the time that the RC oscillator becomes active. If the **NRST** pin is low at the end of this time out, the processor remains in the reset condition until the **NRST** input pin goes high. The user must ensure that input power has risen to a point where the MARC4 can operate properly prior to the time the time delay has elapsed. If there is any doubt, the **NRST** pin should remain low until such time that input power has risen to the minimum operating voltage required. Refer to **Reset modes** in section 2.1 for a detailed description.

1.1.4 TCL, TRM (RC Oscillator)

The system clock for the µC is derived from a fully integrated on-chip RC oscillator circuit. This oscillator tracks the supply and temperature to ensure optimum operation of the microcontroller under all conditions. Normally, the RC oscillator requires no external elements. If it is necessary to trim the frequency up, this may be done by connecting an external resistor in the MΩ range between **TRM** and **V_{INT}**. To measure the resulting RC oscillator/ system clock frequency at the **TCL** pin, **TST1** and **NRST** has to be tied to V_{SS}.

The **TCL** pin can also be used as clock input for an external CMOS oscillator. In this configuration the low power SLEEP mode cannot be used and care must be taken with the reset conditions. The **TCL** pin must be held low for at least 1 ms after the release of power-on or an external reset to allow the external clocking mode.

1.1.5 OSCIN, OSCOUT (Crystal Oscillator)

Normally a 32-kHz standard watch crystal is connected to these pins. A built-in capacitor of 16 to 20 pF can be connected to each of the pads through a program mask option.

Crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start up stabilization time. To ensure proper operation of the crystal oscillator a chosen crystal should follow the standard crystal specification given in table 17.

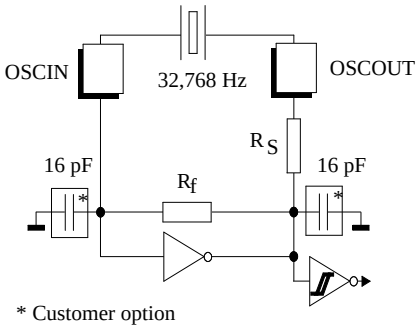


Figure 2. Crystal oscillator

1.1.6 TST1, TST2

These two lines contain integrated Pull-up transistors and define different production and emulation test modes as shown in table 1. During normal operation, connect them to V_{DD}.

Table 1. MARC 4 test mode control

TST1	TST2	TCL	Operation Mode
1	1	N.C. or '1'	Normal mode with internal RC oscillator
1	1	'0' (during POR) clock input	Normal mode with external clock
1	0	'0' (during POR) clock input	Emulation mode with external clock
0	1	System clock output, when µC is active	Oscillator frequency measurement
0	0	Scan clock input	Core scan test mode

1.1.7 I/O Address Map

Table 2 contains the port addresses and a short functional description of the different on-chip peripheral modules.

Table 2. Port address map

Port	Direction	Functional Description
0	I/O	Bidirectional port with pull-up resistors on input and read strobe line OD
1	I/O	Bidirectional port with optional pull-up resistors on input
2	Input	LCD charge pump frequency select (see table 16)
2	Output	LCD control port (see table 15)
3	Input	Watchdog reset
3	Output	LCD data port
4	I/O	Bidirectional port with open drain output as mask option
5	Input	Input port with interrupt facility
5	Output	Key input interrupt1 enable
6	Output	Interrupt and buzzer control port (see table 5)
8	Output	Timer/counter subaddress port (see table 7)
9	Input	Timer/counter capture registers
9	Output	Timer/counter compare registers
10	Output	Watch timer control port (see table 6)

1.1.8 BP00 – BP03 and OD

These four I/O lines and the read strobe line **OD** comprise Port 0. The port consists of CMOS output drivers with integrated pull-up resistors in the input mode. The direction of the port is software programmable and all Port 0 lines are configured as input during power-on or external reset. Refer to the **Input/Output Programming** paragraph for a more detailed description.

1.1.9 BP10 – BP13

These four I/O lines comprise Port 1. The port contains CMOS output drivers with integrated pull-up resistors in the input mode which may be omitted as mask option. The direction of the port is software programmable and all Port 1 lines are configured as input during power-on or external reset. Refer to the **Input/Output Programming** paragraph for a detailed description.

1.1.10 BP40 – BP43

These four I/O lines comprise Port 4. As mask programmable option each I/O line can be used as CMOS or open drain output and with or without an integrated pull-up resistor in the input mode. See figure 6 for a port schematic diagram. The direction of each Port 4 line is bitwise programmable through a data direction control register and all lines are configured as input during power-on or external reset. Additionally, BP40 and BP41 have Schmitt-trigger inputs and can be configured as I/O pins for Timer 0. Those two pins feature high current output drivers to support watch motor applications. BP42 can be selected as buffered frequency output. Refer to the **Input/Output Programming** and **Timer/Counter** paragraphs for more details concerning the programming of Port 4.

1.1.11 IP50 – IP53

These four input lines comprise Port 5. As a mask programmable option each input line can be used with or without an integrated pull-up or pull-down resistor. The Port 5 logic is capable of generating an additional interrupt, when any of the four input lines is activated. The priority level (1 or 4) as well as the active edge are mask programmable options. This function is disabled after power-on or external reset. Refer to the **Input/Output Programming** paragraph for more details.

1.1.12 COM0 – COM3

These four output lines provide the backplane driver signals which should be connected directly to the liquid crystal display unit. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs should not be connected.

1.1.13 S01 – S20

These 20 segment output lines provide the segment driver signals which should be connected directly to the liquid crystal display unit. The segment output signals are generated in accordance with the multiplexed backplane

signals and with the data resident in the display latch. When less than 20 segment outputs are required the unused segment outputs should not be connected.

1.1.14 INT2, INT7 (External Interrupts)

The external interrupt inputs are edge triggered and have Schmitt-trigger characteristics to improve the noise immunity. The active edge is by default the negative edge and both interrupts are enabled after power-on or an external reset, but it may be changed using the interrupt control register accessed through Port 6 (see table 5). See **Interrupts** in section 2.2 for more details.

1.1.15 Buzzer (INT2)

The **INT2** pin is bidirectional. When set to input, this pad functions as an external, maskable interrupt. When set to output the programmer can choose between a static output value or an audio frequency (2 or 4 kHz) square wave. See **Interrupts** in section 2.2 for more details on programming the interrupt control register.

1.1.16 WD_EN, WD_OUT (Watchdog)

In the emulation or I/O test mode, the function of the watchdog timer can be observed at the **WD_OUT** pin.

The functionality of the watchdog is mask programmable in three different ways at the **WD_EN** pad:

- Watchdog is mask disabled: The watchdog function is not available in this configuration.
- Watchdog may be enabled by software: In this case the **WD_EN** pad is configured with an integrated pull-up resistor. The first watchdog read instruction, executed after power-on reset, will start the watchdog timer.
- Watchdog is enabled by hardware: In this mode the **WD_EN** pad is configured with an integrated pull down resistor. After power-on reset, the first watchdog time out happen after the mask selected time, if not reset by a watchdog read access.

1.1.17 TIM1 (Timer 1)

TIM1 is a dedicated bidirectional I/O stage for signal communication to and from the Timer 1 in the timer/counter module (see figure 30). It has no I/O bus interface and is not directly accessible from the CPU. The direction control is performed from the timer/counter configuration registers.

After power-on or external reset, the **TIM1** pin is set to input mode, configured for external clock input and interrupt disable. See **Timer/Counter** in section 4 for more details on programming.

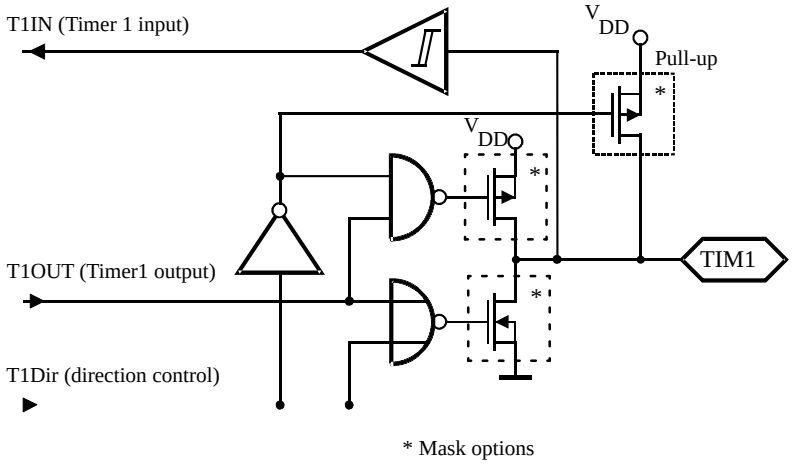


Figure 3. Bidirectional pin TIM1

1.2 Input/Output Programming

1.2.1 Bidirectional Port 0 and Port 1

Port 0 and 1 may be programmed as an input or an output under software control. The direction of a port is determined by an IN or OUT instruction and is held until another IN or OUT instruction for this port is executed.

The direction of bidirectional Port 0 and Port 1 are switchable on a nibble-wise basis only. The output latches hold the state of the last data value written to the port. At power-on or external reset all pins of Port 0 and 1 are set to input mode and all output latches are set to a logic 1. Whenever a bidirectional port is switched from input to output the last value stored in the latches will appear on the outputs for one clock cycle (see figure 5).

When switching bidirectional ports from output to input the stray capacitance of the connection wires may cause the data read to be the same as the last data written to this port. This behaviour can be used by connecting large enough capacitors to the pins of the bidirectional port to read back the previous data written to this port.

On the other hand, to avoid the negative effects of stray capacitances one of the following approaches should be used:

- Use two IN instructions, and DROP the first data nibble read.
- Write a logic '1' to the port bits to be read before executing the IN instruction.

The **OD** signal is a strobe output indicating that data is being read from Port 0 by the µC. Data must be valid at the latest 100 ns after the falling edge of **OD**.

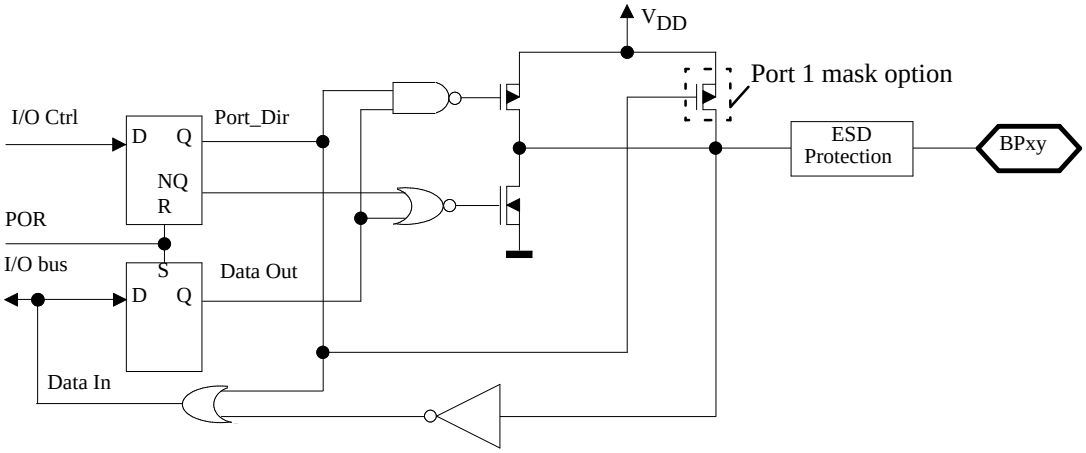
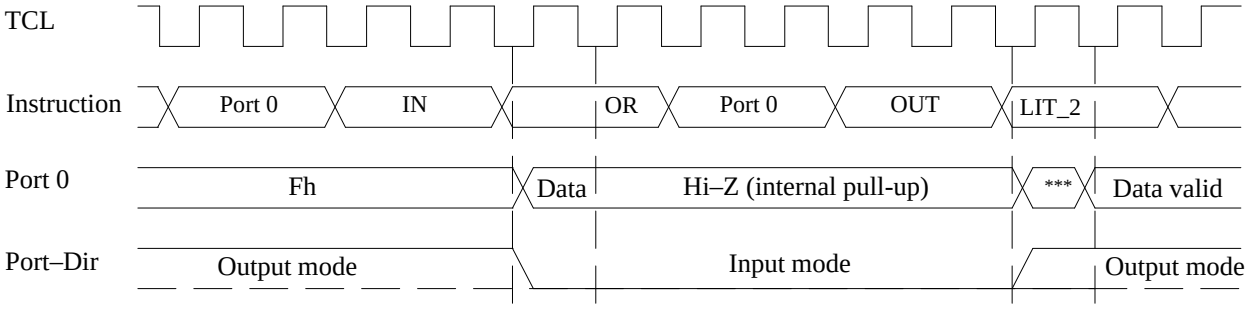


Figure 4. Bidirectional Port 0 and 1 schematics



***) Last written data contained in output latches, Fh after power–on reset

Figure 5. Port read and write cycle timing

1.2.2 Bidirectional Port 4

Port 4 may be programmed as an input or an output under software control. The direction of the port (in native mode) is determined by an IN or OUT instruction and is held until another IN or OUT instruction for Port 4 is executed. As mask programmable option each I/O line can be used as CMOS or open drain output and with or without an integrated pull-up resistor in the input mode. See figure 6 for a port schematic diagram. The direction of each Port 4 line is bitwise programmable through a data direction control register (P4DDR) and all lines are configured as input during power-on or external reset. Additionally BP40 and BP41 have Schmitt-trigger inputs and can be configured as I/O pins for Timer 0. BP42 can be selected as buffered frequency output. See tables 13 and 14 in the **Timer/Counter** section for more details on Port 4 special function register control.

1.2.3 Input Port 5

The data on Port 5 is sent to the top of the expression stack whenever an IN instruction (addressing Port 5) is executed. The Port 5 logic may generate an additional interrupt with mask selectable priority level 1 or 4, when any of the four input lines is driven low. This function is useful for implementing an interrupt driven keyboard. It is disabled after power-on or external reset. The corresponding interrupt is enabled by writing any value to Port 5 and automatically disabled after a read operation from Port 5. The interrupt service routine may use the 2nd watch timer to perform a software based key debouncing. Note: The data read from input pins with an integrated pull-down resistor are inverted (e.g. if 1011b is read, data at IP5 is 0100b).

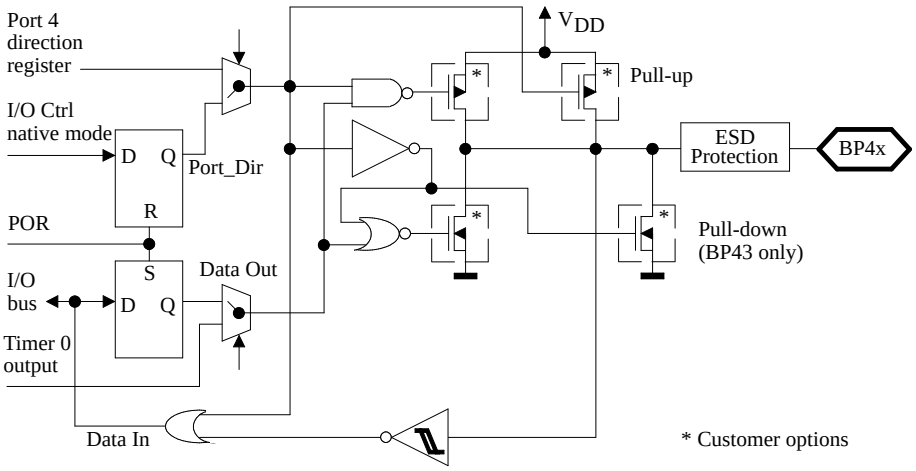


Figure 6. Bidirectional Port 4 schematics

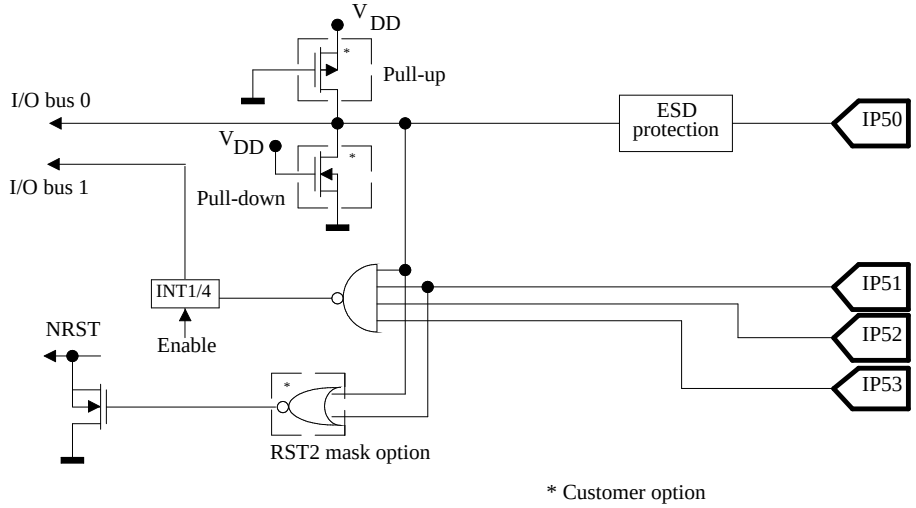


Figure 7. Port 5 with pull-up and RST2 mask option

1.3 Memory

The MARC4 family of microcontrollers is based on the Harvard architecture with physically separate program memory (ROM) and data memory (RAM).

The program memory (ROM) is mask programmed with the customer application program during the fabrication of the microcontroller. The ROM is addressed by a 12-bit wide program counter, thus limiting the program size to a maximum of 4,096 bytes. The user ROM starts with a 512 byte segment (’Zero Page’) which contains predefined start addresses for interrupt service routines and special subroutines accessible with single byte (SCALL) instructions. The corresponding memory map is shown in figure 8.

The self test routines have to be included as part of the free program space. The 16-bit check sum (CRC) is located by the compiler in the last two bytes of ROM.

The on-chip 256 x 4-bit RAM is divided in the 12-bit wide return stack, the 4-bit wide expression stack (both with a user definable depth) and the data memory. The fixed return address (000h) which points to the $AUTOSLEEP routine is located at RAM address FCh.

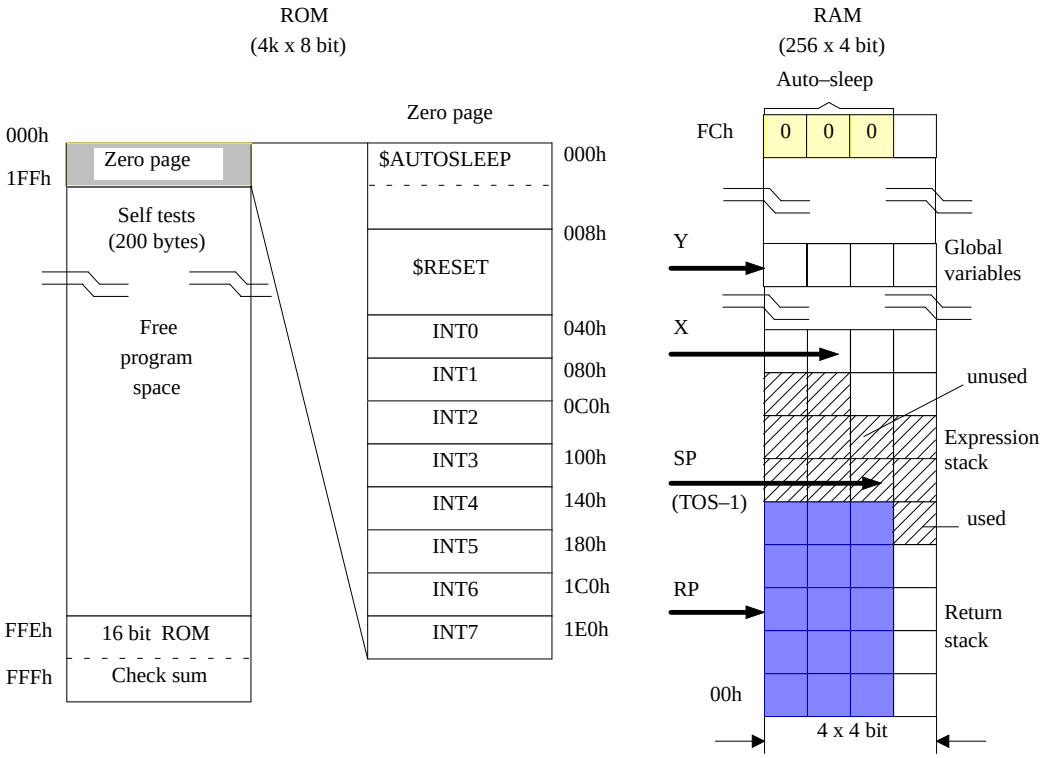


Figure 8. Memory map

1.4 Core registers

As shown in the register set below, the MARC4 core has seven registers.

1.4.1 Accumulator (TOS)

Because this microcontroller is a stack based machine with two on-chip stacks located in the internal RAM, all arithmetic, I/O and memory reference operations take their operands from, and return their result to the 4-bit wide expression stack. This stack is also used for passing parameters between subroutines, and as a scratchpad area for temporary storage of data. The top element of the expression stack is immediately accessible through the TOS register. The MARC4 can perform most of the operations dealing with the top of stack items (TOS and TOS-1) in a single byte, single cycle instruction.

1.4.2 Expression Stack Pointer (SP)

The 8-bit wide stack pointer **SP** contains the address of the next-to-top 4-bit item (TOS-1) on the expression stack, located in the internal RAM. After power-on reset the stack pointer has to be initialized to the start address of the allocated expression stack area (**S0**).

1.4.3 RAM Address Register (X and Y)

The 8-bit wide registers **X** and **Y** are used to address any 4-bit item in the RAM. Using either the pre-increment or post-decrement addressing mode it is comfortable to compare, fill or move arrays in the RAM area.

1.4.4 Return Stack Pointer (RP)

The return stack pointer **RP** points to the top element of the return stack. The 12-bit wide return stack is used for storing subroutine return addresses and keeping loop index counts. The return stack can also be used as a temporary storage area. The MARC4 instruction set supports the exchange of data between the top elements of the expression and return stack. The return stack automatically pre-increments and post-decrements in steps of 4. This means that every time a subroutine return address is stacked, 4-bit RAM locations are left unwritten. These locations are used by the qFORTH compiler to allocate 4-bit variables. After power-on reset the return stack pointer has to be initialized to FCh.

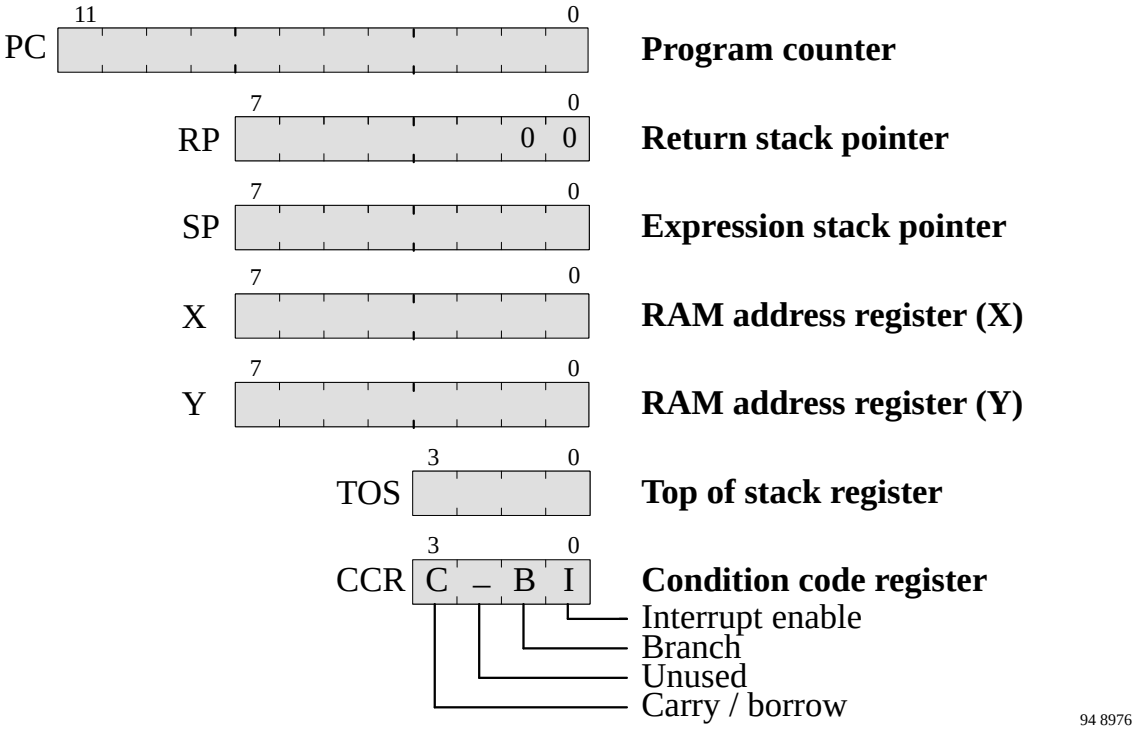


Figure 9. Programming model

1.4.5 Program Counter (PC)

The program counter (PC) is a 12-bit register that contains the address of the next instruction to be executed by the microcontroller. After power-on or external reset the program counter is set to address 008 by the reset vector.

1.4.6 Condition Code Register (CCR)

The 4-bit wide condition code register (CCR) indicates the results of the instruction just executed as well as the state of the microcontroller. These bits can be individually tested by a program and specified action will take place as a result of their state. Each bit is explained in the following paragraphs.

- **Carry/Borrow (C)**
  This flag indicates that a borrow or carry out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during shift and rotate operations and the execution of SET_BCF, CLR_BCF and CCR! instructions.
- **Zero (Z)**
  When this bit is set, it indicates that the result of the last arithmetic or logical manipulation was zero.
- **Branch (B)**
  A conditional branch takes place when the branch flag was set by one of the previous instructions (e.g. a comparison operation). Instructions such as SET_BCF, TOG_BF, and CLR_BCF allow the direct manipulation of the branch flag under program control. The branch flag is affected by all ALU operations except CCR@, DI, SWI, RTI, and OUT.
- **Interrupt enable (I)**
  This flag is used to control the interrupt processing on a global basis. Resetting the interrupt enable flag (using the DI instruction) disables all interrupts. The µC does not process further interrupt requests until the interrupt enable flag is set again by either executing an EI, RTI (Return-from-interrupt) instruction or entering the SLEEP mode. After power-on or an external reset the interrupt enable flag is automatically reset. The RTI instruction at the end of the $RESET routine will set the interrupt enable flag and thereby enable all interrupts.

1.4.7 Self-Check

The self test capability of the MARC4 provides the possibility of easily checking the core by executing the RAM and ROM tests after power-on reset. These selftest routines must be included either conditionally or unconditionally in the $RESET routine after the initialization of the stack pointers.

If the self test routines are included unconditionally care should be taken that the pattern written to Port 1 does not interfere with the application hardware. If the stimulus read from Port 0 is different from zero, TEMIC Semiconductors has to be informed. Please use the ordering information on the last page of this data sheet.

Please contact your local TEMIC Application Engineer for the correct installation and optimization of the self test routines.

2 Reset Modes, Interrupts, and Low Power Modes

This chapter descripes the reset modes and the different interrupt capabilities of this microcontroller. The low power consumption modes are also discussed.

2.1 Reset Modes

The M44C636 has four reset modes: an active low external reset pin (**NRST**), a power-on reset function, a coded reset at Port 5 and a watchdog time-out. These reset modes guarantee a well-defined start up condition of the complete microcontroller. During any hardware reset all interrupts are disabled, all pending and active interrupts are cleared, all on-chip peripherals are reset and a non-maskable interrupt request is generated. After execution of the reset service routine the interrupts are enabled automatically by the RTI or a previously executed EI instruction.

2.1.1 External Reset (NRST)

The **NRST** input pin is used to reset the µC to provide an orderly software start-up procedure. When using the external reset, the pin **NRST** should be held low for a minimum of 10 µs.

2.1.2 Power-on Reset

A power-on reset occurs when a positive transition is detected on the power supply input pin. For a proper operation of this circuitry an external capacitor of 0.47 to 2.2 µF is recommended on the **NRST** pin, if the circuit is operated at voltages below 1.5 V.

2.1.3 Coded Reset at Port 5

Another way of invoking an external reset mode is to force an active low (high) signal simultaneously to some of the Port 5 input lines (IP50 to IP53) selected by mask option. Table 3 shows the combination of input lines that can be selected by mask option.

Table 3. Multiple key reset options

NO_RST	Not used (default)
RST2	IP50 & IP51
RST3	IP50 & IP51 & IP52
RST4	IP50 & IP51 & IP52 & IP53

When, for instance, mask option RST2 (IP50 & IP51) is selected, an external reset is executed when the signal inputs to these two lines are both activated at the same time.

If this function is used, it is essential that the specified input lines are not activated at the same time during normal operation in the application. The activation voltage level (V_{SS} or V_{DD}) depends on the selected Port 5 pull-up/ pull-down option setting.

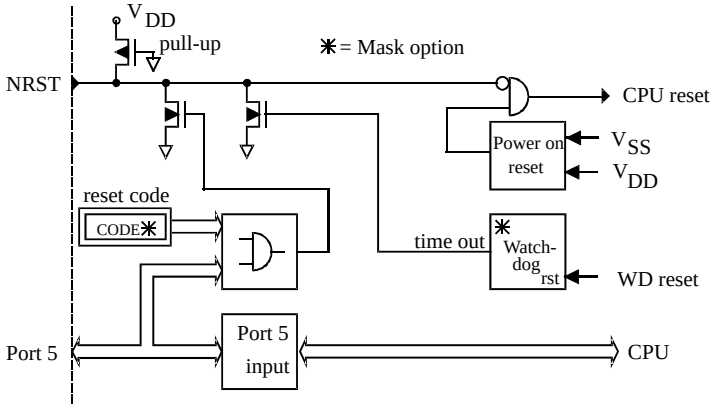


Figure 10. Reset configuration

2.1.4 Watchdog Timer

The purpose of the watchdog timer is to detect the malfunction (runaway) of the program due to external noise or other causes and return the operation to the normal condition.

The watchdog timer is a 17 stage divider clocked from the 32-kHz SUBCL clock (see figure 11). It can be enabled as a mask option either automatically after power-on reset (WD_EN with internal pull down) or by software after the first watchdog read access (WD_EN with internal pull

down resistor). By default, the watchdog timer will be disabled through a pull-up resistor at WD_EN. If enabled it must be periodically reset from the application program. The program cannot disable the watchdog. Should for any reason, the CPU find itself for an extended period in SLEEP or in a section of program that includes no watchdog reset, then the watchdog will overflow, thus forcing the NRST pin low. This in turn initiates a master reset. The timeout period can be set to 0.5, 1 or 2 seconds as a mask option.

To reset the watchdog the program must perform an IN instruction on the address WDRES ('3' hex). No relevant data will be received, so this operation will normally followed by a DROP to flush the data from the stack.

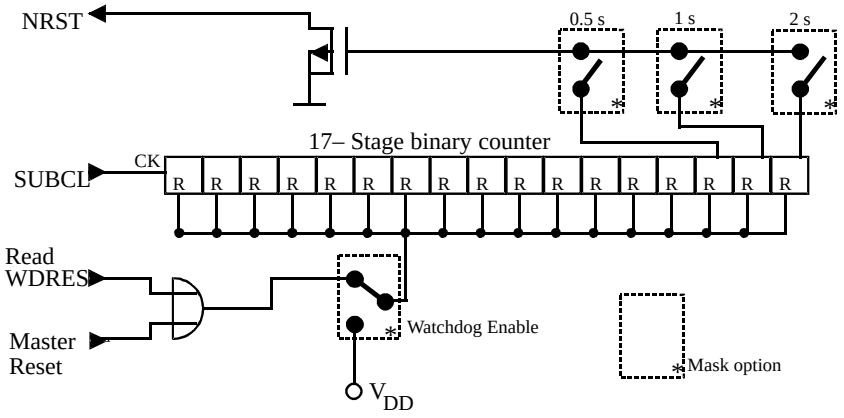


Figure 11. Watchdog timer

2.2 Interrupts

The MARC4 can handle interrupts of up to 8 priority levels (Table 4). They are generated from on-chip modules (timer/counters, watch timer), external sources (Port 5 inputs, interrupt pads) or synchronously from the core itself (software interrupts). Each interrupt source has a hard-wired interrupt priority and an associated interrupt service routine in the program ROM. The programmer can enable or disable all interrupts by setting or resetting the interrupt enable flag in the CCR using the EI or DI instruction.When the interrupt enable flag is reset (interrupts disabled), the execution of interrupts is inhibited but not the logging of the interrupt requests in the interrupt pending register. While interrupts are disabled (e.g. for a time critical section of code) and an interrupt is generated the interrupt will not be lost. Its execution will only be delayed until interrupts are enabled again. Interrupts are only lost when the pending register for a particular interrupt priority is still set at the time of a further interrupt transmission of the same level. The pending register is cleared on any hardware reset. On completion of an interrupt service routine the corresponding pending and active bits are cleared by executing the RTI instruction (see figures 12 and 13).

The µC automatically enters the SLEEP mode when the lowest priority interrupt service routine has been completed. This guarantees a maximum use of the power saving capabilities of the µC. Refer to **Low Power Modes** for more information.

Table 4. Interrupt priority and address allocation map

Priority	Function	Located in ROM at	Max. Length [ROM bytes]	Interrupt Opcode
INT7	External hardware interrupt INT7, negative/positive edge triggered	1E0h	≥24	FCh
INT6	Watch timer interrupt, high frequency	1C0h	32	F8h
INT5	Watch timer interrupt, low frequency	180h	64	F0h
INT4	Timer/Counter 0 (or Port 5 interrupt)	140h	64	E8h
INT3	Timer/Counter 1	100h	64	E0h
INT2	External hardware interrupt INT2, negative/positive edge triggered	0C0h	64	D8h
INT1	Port 5, key input interrupt	080h	64	D0h
INT0	Software interrupt (SWI0)	040h	64	C8h

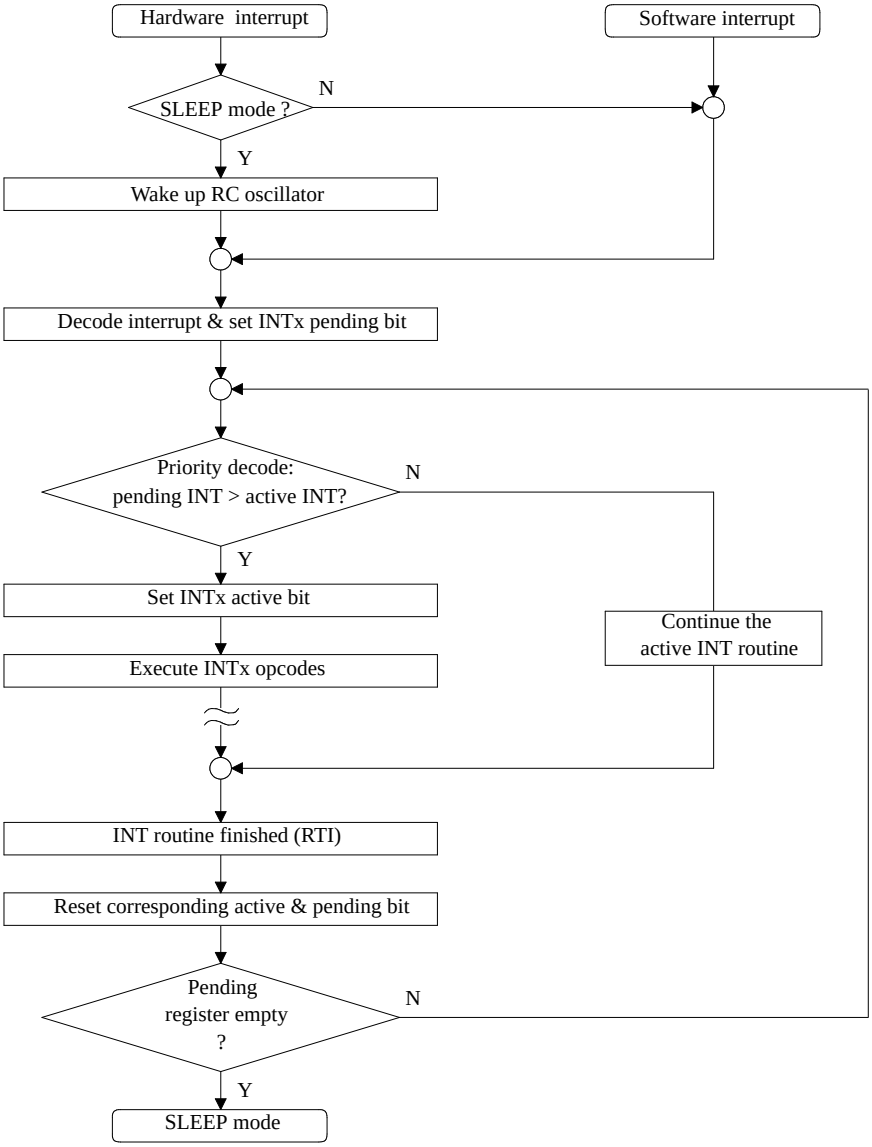


Figure 12. Interrupt flowchart

2.2.1 Interrupt Handling

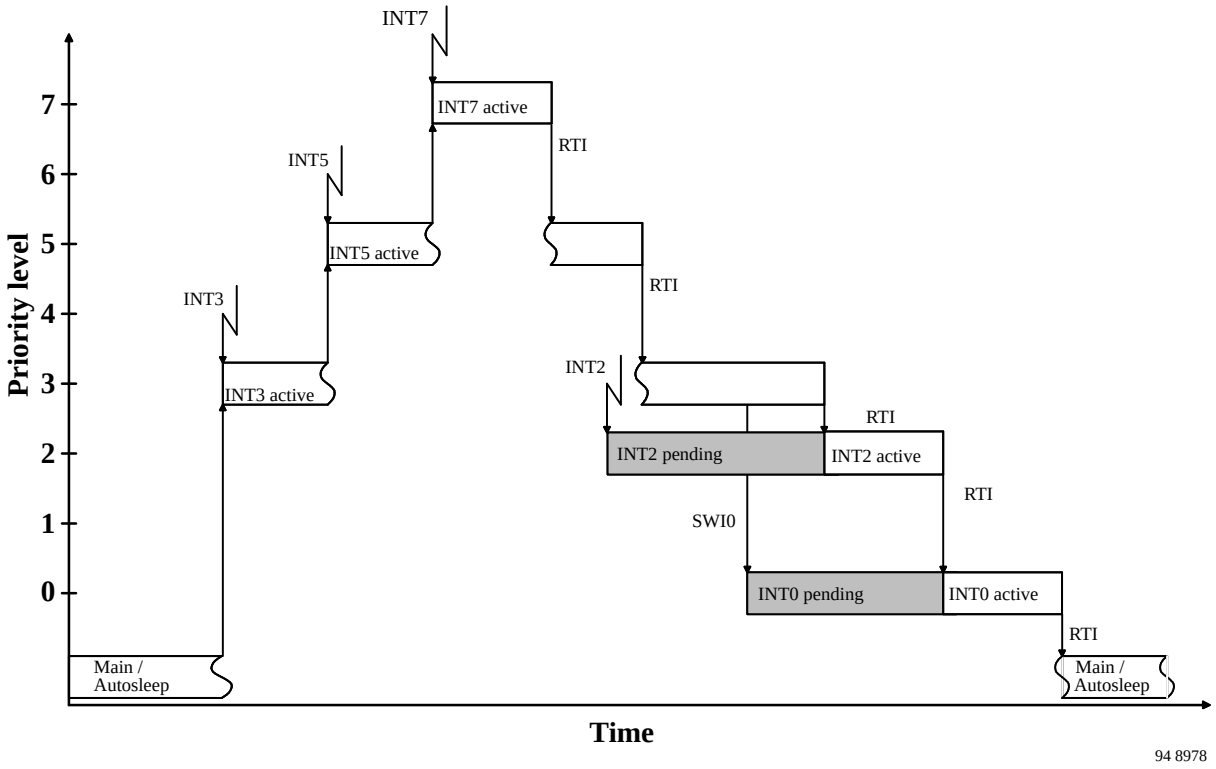


Figure 13. Interrupt processing

The integrated interrupt controller samples all interrupt requests and latches these in the interrupt pending register. It also decodes the priority of the interrupt requests, and signals the µC when a higher priority interrupt request is present. If the µC (with interrupts enabled) receives the interrupt controller's signal an interrupt acknowledge cycle will be entered. During this cycle, the µC saves the current PC on the return stack and loads the PC with the start address of the corresponding interrupt service routine. When the µC is in the SLEEP mode it will be activated by any hardware interrupt, by the means of starting the RC oscillator and decoding the interrupt. By using the MARC4 way of interrupt transmission it is possible to transmit more than one interrupt at the same time. The transmitted interrupts are loaded into the interrupt pending register asynchronously. The priority decoder determines the interrupt with the highest priority and activates it as shown in figure 12. The interrupt priority level handling versus time is shown in figure 13.

2.2.2 Interrupt Latency

The interrupt latency is the time from the transmission of the interrupt to the interrupt service routine being activated. This time is at minimum three and at maximum five instruction cycles depending on the state of the core. The highest interrupt frequency which can be reasonably handled is 1 kHz depending on the supply voltage range (i.e. the RC oscillator frequency) and the duty cycle of the application.

2.2.3 Software Interrupts

Software interrupts are executable instructions which are supported by predefined macros named SWI0 through SWI7. The software triggered interrupt operates exactly like any hardware triggered interrupt.

2.3 Hardware Interrupt Sources

2.3.1 Port 5 Interrupt

The input Port 5 may generate an interrupt (of masked priority level 1 or 4) if any of the four input lines of Port 5 is activated. The active interrupt edge depends on the mask option for the intergrated Port 5 pull-up (negative egde) or pull-down resistor (positive edge). This function is disabled after power-on reset or external reset. The interrupt is enabled by writing any value to Port 5 and is automatically disabled after a read from Port 5.

2.3.2 External interrupt inputs INT2 and INT7

The external interrupt inputs are edge triggered and have Schmitt-trigger characteristics to improve the noise immunity. The active edge is by default the negative edge, but it may be changed using the interrupt control register accessed through Port 6 (see table 5). The microcontroller completes the current instruction before it responds to the interrupt request. When the interrupt input pin recognizes an active edge, a logic one is latched internally to signify the interrupt request, if the corresponding enable bit in the mask register is set. Then the microcontroller completes its current instruction and the interrupt pending register is tested. If an interrupt is pending and the interrupt enable bit in the condition code register is set, the interrupt sequence begins. As shown in figures 14 and 15, the following mask programmable options are available on the two external interrupt input pads:

- Integrated pull-up
- Integrated pull-down
- No pull-up or pull-down
- Buzzer as CMOS or open drain output (INT2 only)

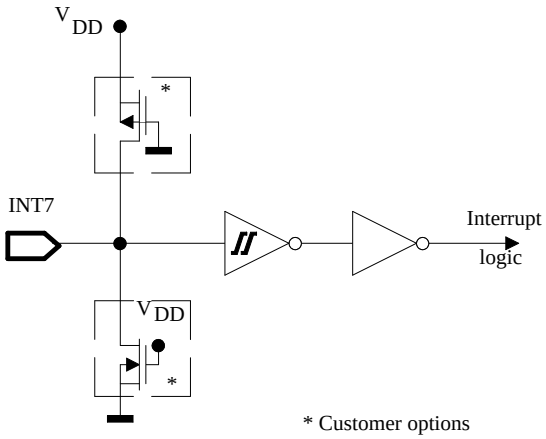


Figure 14. External interrupt INT7

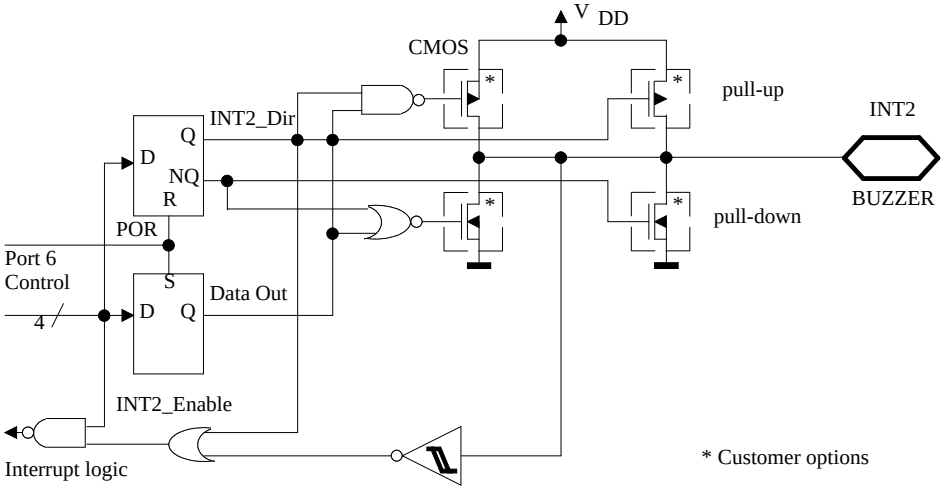


Figure 15. External interrupt INT2 and BUZZER output

2.3.3 Buzzer and Interrupt Control Register

The two external interrupt inputs **INT2** and **INT7** are maskable. This means **INT2** or **INT7** may be disabled individually while still receiving all other interrupts. After any hardware reset both interrupt inputs are enabled and are negative edge triggered, which corresponds to control code Fh. Additionally, if not used as an interrupt input, **INT2** can be utilized as an output. A static output level or an audio frequency square wave is selectable in output mode. The tone frequency is derived from the crystal oscillator frequency f_C and can be easily calculated by the following formula:

$$f_{BUZZER} = \frac{f_C}{2^3} \text{ or } \frac{f_C}{2^4}$$

The frequency is software programmable to either 4,096 kHz or 2,048 kHz (if a standard watch crystal is used). See section 4.2.3 for more details on the buzzer frequency toggle function. This output mode may also be useful for trimming the crystal oscillator frequency. All

of these interrupt control functions are selected by writing a control nibble to Port 6 (see table 5).

Table 5. Interrupt control register (Port 6)

Control Code	INT7, Active Edge	INT2, Active Edge	INT2 I/O Function
1111	enabled, negative edge	enabled, negative edge	Interrupt input
1110	enabled, negative edge	enabled, positive edge	Interrupt input
1101	enabled, positive edge	enabled, negative edge	Interrupt input
1100	enabled, positive edge	enabled, positive edge	Interrupt input
1011	enabled, negative edge	masked, negative edge	Interrupt input
0111	masked, negative edge	enabled, negative edge	Interrupt input
0011	masked, negative edge	masked, negative edge	Interrupt input
1010	enabled, previous progr.	masked, previous progr.	Output high
1001	enabled, previous progr.	masked, previous progr.	Output low
1000	enabled, previous progr.	masked, previous progr.	Buzzer frequency output
0010	masked, previous progr.	masked, previous progr.	Output high
0001	masked, previous progr.	masked, previous progr.	Output low
0000	masked, previous progr.	masked, previous progr.	Buzzer frequency output

2.3.4 Watch Timer Interrupts

The programmable watch timer is usually driven by an external 32.768 kHz watch crystal. Using for example a 38.4 kHz crystal, it is possible to emulate an asynchronous serial interface protocol using standard baud rates by software.

The watch timer module consists of a 15 stage divider chain with two multiplexers. They offer two interrupt sources with priority level 5 and 6. The watch timer powers up in the reset condition which corresponds to control code Fh. The basic watch timer interrupt (INT5) has 8 programmable frequencies from 128 Hz down to 1 Hz. They can be selected by writing the value 7 to 0 into the control register at port address 15. The corresponding interrupt (**INT5**) can only be masked by resetting the complete watch timer module.

Table 6. Interrupt interval times for the watch timer

Control Code	Interrupt Source	Interrupt Frequency	f_C = 32.768 kHz	
			Time Interval	Interrupt Frequency
F	none	Reset & hold complete prescaler		
E	(INT5 only)	INT6 disabled, INT5 still active		
D	INT6	$f_C/2^3$	244.14 µs	4,096 Hz
C	INT6	$f_C/2^5$	976.56 µs	1,024 Hz
B	INT6	$f_C/2^7$	3.906 ms	256 Hz
A	INT6	$f_C/2^9$	15.625 ms	64 Hz
9	INT6	$f_C/2^{11}$	62.5 ms	16 Hz
8	INT5	reserved		
7	INT5	$f_C/2^8$	7.81 ms	128 Hz
6	INT5	$f_C/2^9$	15.625 ms	64 Hz
5	INT5	$f_C/2^{10}$	31.25 ms	32 Hz
4	INT5	$f_C/2^{11}$	62.5 ms	16 Hz
3	INT5	$f_C/2^{12}$	125 ms	8 Hz
2	INT5	$f_C/2^{13}$	250 ms	4 Hz

1	INT5	$f_C/2^{14}$	500 ms	2 Hz
0	INT5	$f_C/2^{15}$	1 s	1 Hz

The second interrupt source (INT6) allows the selection of 5 different frequencies from the divider chain ranging from about 4 kHz down to 16 Hz by writing the corresponding code (Dh to 9) into the control register at port address 15. The interrupt **INT6** may be disabled selectively using control code Eh without affecting the interval time programming of **INT5**. The **INT6** multiplexer powers up in the disabled position. The programming of the **INT6** interrupt tabs should be done synchronously, if different time base intervals are used temporarily (stop watch application, keyboard debouncing) or an accurate number of interrupts is required. To avoid the transmission of additional unwanted interrupts, the change of the **INT6** interval times should be done in a time frame of 200 µs after the reception of a watch timer interrupt. As illustrated in table 6 only the **INT6** timer can be disabled individually. Therefore special care has to be taken for **INT5**. In the case of programming the **INT6** timer without previously selecting an **INT5** frequency (i.e. after power-on reset), a **INT5** frequency of 128 Hz is set by default. Concerning the program development using **INT6**, the following rules should be considered:

- Always program both interrupt multiplexers of the watch timer module,
- If only **INT6** is required, select the 1 Hz tab first and define an empty **INT5** routine,
- Otherwise implement a 'disable' flag in the **INT5** service routine.

2.3.5 Timer/Counter Interrupts

The Timer 1 generates (if enabled) an interrupt of priority level 3 (INT3) on every match with the data byte which was written into the Timer 1 compare register (T1CA). On the other hand the interrupt generation (INT4) of Timer 0 is controlled by the selected mode of operation. This means, Timer 0 modes based on a free running counter will generate an INT4 (if enabled) on every overflow ($f_{IN}/256$), whereas modes with a reload function generate the interrupt with the compare match. See section **Timer/ Counter Module** for further details.

2.4 Low Power Modes

Three low power consumption modes are available: SLEEP, power saving and STOP mode. These operating modes are all initiated by executing the SLEEP instruction.

Note 1: The SLEEP instruction is not a normal instruction as its function is dependent on the state of the interrupt pending register. SLEEP is therefore available for use within the $AUTOSLEEP routine or $RESET routine only.

Note 2: If a timer/counter is operating with the system clock (VALIDATE) as input source, the SLEEP mode will stop the input clock. Therefore keep the µC conditionally busy as long as the PWM mode is needed.

2.4.1 SLEEP Mode

By executing the SLEEP instruction either in the $AUTOSLEEP function or during power-on reset in the initialisation routine, the microcontroller enters a low power consumption mode. In this SLEEP mode, the programmable timers and the LCD driver remain active, while the internal RC oscillator (µC clock) is turned off causing all core processing to be stopped. It can only be kept when none of the interrupt pending or active register bits are set.

During the SLEEP mode, the interrupt enable flag in the condition code register is set to enable all interrupts. All other registers, memory, and parallel input/output lines remain the same. The 32-kHz crystal oscillator is not switched off, but the timers or the LCD driver may be disabled by the application program. This mode will continue until any interrupt or reset is sensed. At this time the event is decoded and the program counter is loaded with the corresponding starting address of the interrupt or reset service routine.

The MARC4's unique **Auto-Sleep** feature allows the µC to enter the SLEEP mode automatically when the lowest priority interrupt service routine has been completed.

The SLEEP mode is a shutdown condition which is used to reduce the average system power consumption in applications where the µC is not fully utilised (figure 16). Using SLEEP and interrupts, the full computational speed of the core is always available. In this way, power is only consumed when needed, allowing the µC to run in high speed bursts from a weak supply (battery, capacitor, or even a solar cell). When **TST1** is tied to $\mathbf{V_{SS}}$ after power-on reset, the µC activity is observable at the **TCL** pin.

Calculating the average power consumption

The total power consumption is directly proportional to the active time of the µC. For a rough estimation of the expected average system current consumption, the following formula should be used:

$$I_{SYS} = I_{SLE} + \left(I_{DD} \cdot \frac{T_{active}}{T_{total}} \right)$$

The duty cycle of the µC can also be observed in a MARC4 emulator window and with the target application board in stand alone operation.

2.4.2 Power Saving Mode

The power saving feature of the LCD driver in conjunction with the SLEEP mode of the core will further reduce the system power consumption by additionally blanking the LCD. This is done by disabling the LCD voltage generator and switching all LCD voltage levels to V_{SS}, thus causing a reduction in display power consumption. This mode is only effective if the display is generally to be blanked for periods longer than 5 seconds. Refer to section 4 for more information on LCD driver programming.

2.4.3 STOP Mode

The lowest power consumption mode of the microcontroller is entered with the STOP operation. The current consumption of the µC (without external loads) will be reduced to less than 100 nA at 1.5 V.

The STOP mode can be implemented by switching off the power supply of the crystal oscillator (**AV_{DD}**) with one of the port output lines. Before executing the STOP routine, the prescaler should be reset and the LCD driver should be put into the power saving mode, because both are turned off when the 32-kHz oscillator is switched off. The internal RC oscillator is stopped by the SLEEP instruction, suspending all further internal processing.

During the STOP mode, the interrupt enable flag in the CCR is set to enable external interrupts. All other registers, memory, and all I/O lines remain unchanged. This continues until an external interrupt or reset is decoded. The program counter is loaded with the corresponding starting address of the interrupt or reset service routine respectively.

By writing a logic 1 to the corresponding port, the interrupt or reset service routine may turn on the crystal oscillator. The oscillator's start up time in the range of 1 to 2 seconds (which depends on the operating temperature and supply voltage) must be kept in mind. Therefore the occurrence of the first timer interrupts might not be as accurate as usual.

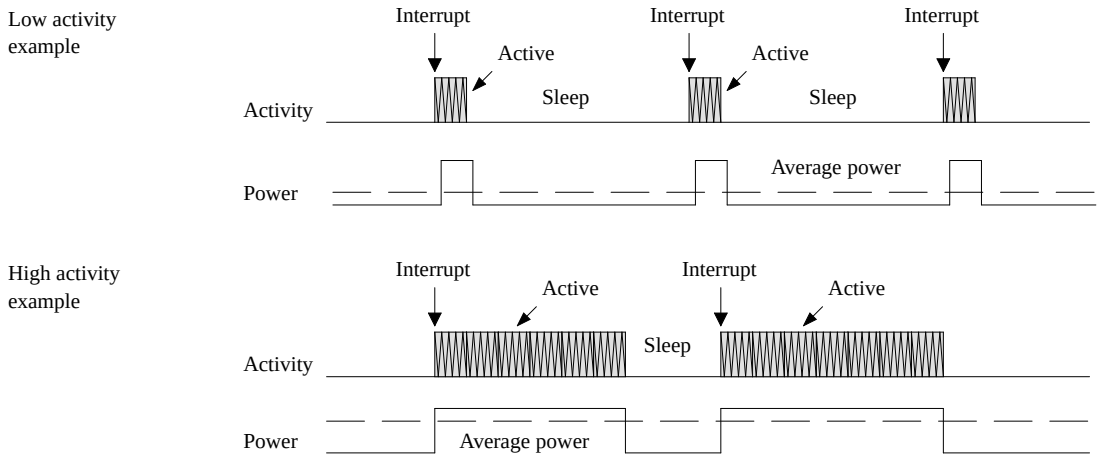


Figure 16. Average system power consumption and duty cycle

3 Timer/Counter Module

The M44C636 has two programmable 8-bit timer/ counter, which can be configured as one 16-bit timer/counter. Each timer is preceded by an additional 8-bit partly programmable input clock prescaler. The clock source is individually user selectable for Timer 0 and Timer 1 out of eight different input signals. This is controlled by the Timer 0 and Timer 1 control registers T0CR and T1CR. The implemented features allow various operating modes such as period measurement, pulse width modulation (PWM), pulse density modulation (PDM), phase shift measurement, position measurement and also usual timer modes like event counting and auto reload function. Interrupts are generated, if enabled in the T0CR and T1CR register at various timer events. Block diagrams of the timers are shown in figures 18 and 30.

All timer/counter registers are accessible by writing the specific register address to the timer subaddress register TSUB (Port 8) and the data to the timer data port (Port 9). Because of the 8-bit architecture of the timer/counter module, each capture and compare register is represented by two nibbles (higher and lower). Generally, for a write operation first the lower and then the higher nibble is written, whereas the higher nibble is accessed first for a read operation. The timer interrupt generation is inhibited until both nibbles are written into the compare register. Timer data can be read at any time and timer/counter operation is not disturbed whilst reading.

The timer capabilities are provided by using the following control registers.

Table 7. Timer/counter subaddress register TSUB (Port 8)

Timer/Counter Register		Name	I/O	Function Register
0	0000	T0MO	Out	Timer 0 mode register
1	0001	T0CR	Out	Timer 0 control register
2	0010	T1MO	Out	Timer 1 mode register
3	0011	T1CR	Out	Timer 1 control register
4	0100	TCMO	Out	Timer/counter mode register
5	0101	P4IOR	Out	Timer 0 and port4 I/O control register
6	0110	P4DDR	Out	Port 4 data direction control register
7	0111		–	reserved
8	1000	T1CP	Out	Timer 1 – 8-bit compare register
8	1000	T1CA	In	Timer 1 – 8-bit capture register
9	1001	T0CP	Out	Timer 0 – 8-bit compare register
9	1001	T0CA	In	Timer 0 – 8-bit capture register

3.1 Timer/Counter I/O Addressing

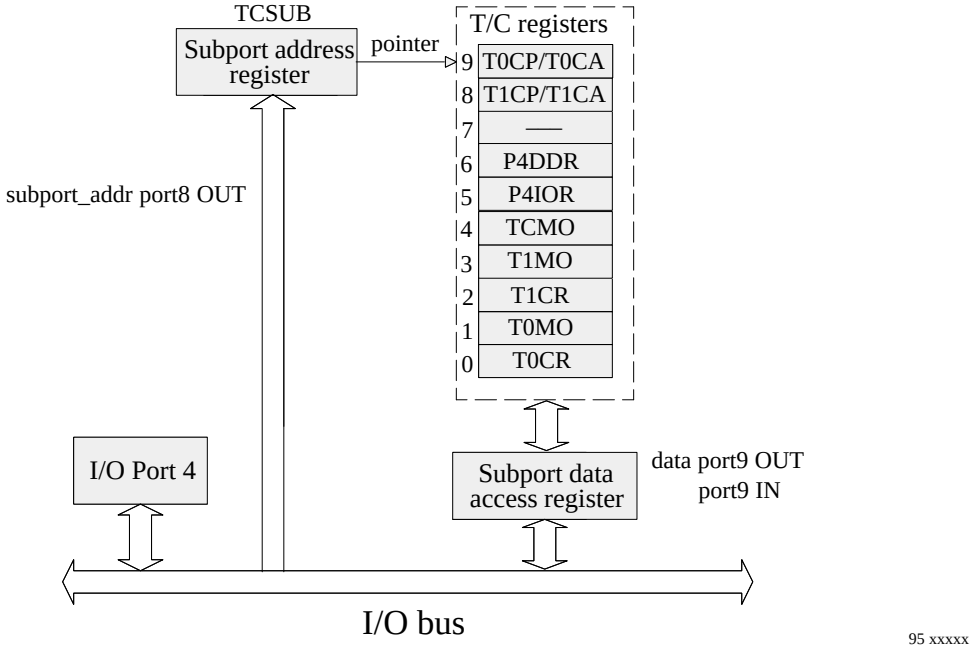


Figure 17. Timer/Counter extended I/O addressing

To address a timer/counter register, first of all, the subport address register TCSUB (Port 8) has to be initialised. Afterwards the appropriate data can be written (or read) via the subport data access register (Port 9).

Example:

Setup Timer 0 for frequency measurement mode with a 32 kHz sampling frequency

```
0       CONSTANT            T0MO
        1111b CONSTANT      T0_Freq_measure
1       CONSTANT            T0CR
        0000b CONSTANT      Fin_32kHZ_EI
4       CONSTANT            TCMO
        0110b CONSTANT      T0_Start
        0111b CONSTANT      TC_Start
5       CONSTANT            P4IOR
        0101b CONSTANT      P41=T0IN1
9       CONSTANT            T0CA                    \ T9 capture register

\       TC_Ctrl writes one control nibble to a T/C register

        : TC_Ctrl           ( TC_data TC_subport — )
          Port9 SWAP
          Port8 OUT OUT
        ;
```

```
\       Initialising Timer 0

        T0_Freq_Measure         T0MO  TC_Ctrl
        Fin_32kHz_EI            T0CR  TC_Ctrl
        P41=T0IN1               P4IOR  TC_Ctrl
        T0_Start                TCMO  TC_Ctrl

\       Read–out of T0 capture register

        : T0_CA_Read
                                DI
                                T0CA  Port8  OUT
                                Port9  IN               \ Read higher nibble
                                Port9  IN               \ Read lower nibble
                                EI
        ;

\       Timer 0 interrupt service routine

        : INT4                  T0_CA_Read
                                New_Freq  2!            \ Save T0 result
        ;
```

3.2 Timer/Counter 0

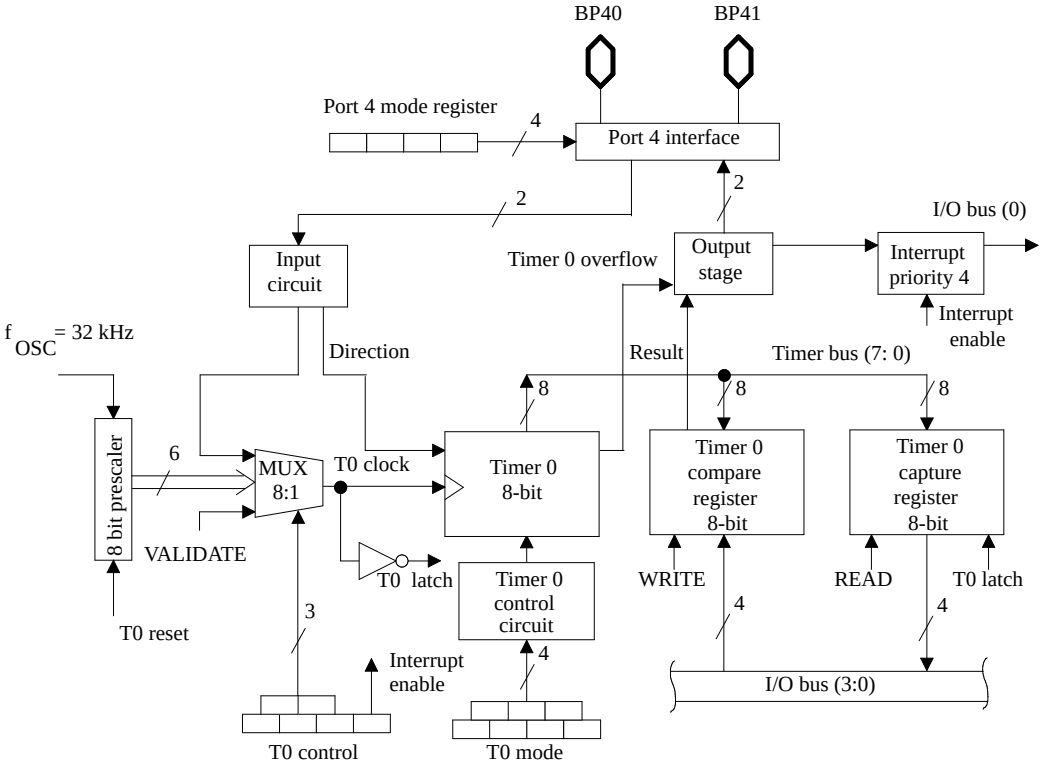


Figure 18. Timer 0 block diagram

Timer 0 is a synchronous up/down counter. The down counting mode is not user programmable but in the position measurement mode the Timer 0 input circuit generates a direction signal for up/down counting. Depending on the programmed timer/counter mode an interrupt in the T0MO register, of priority level 4 is generated either at a timer/counter overflow or a successful compare result of the timer count value and the Timer 0 compare register T0CP.

Timer 0 shares its two I/O pins with Port 4 (BP40, BP41). The Port 4 interface circuit can be configured by the Port 4 I/O control register P$IOR. This register must be programmed when the timer/counter is driven by external signals or external hardware by timer/counter signals. The timer I/O pin direction is automatically controlled by the hardware.

3.3 Timer 0 Modes

The various operating modes of Timer 0 (see table 8) are selected through the Timer 0 mode register T0MO at subaddress 0. For a more detailed description of these modes see the following paragraphs.

Timer 0 Mode Register (T0MO)

Subport address: ’0’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T0MO	**T0MO3**	**T0MO2**	**T0MO1**	**T0MO0**	**Reset value: 1111b**

Table 8. Timer 0 mode register T0MO

3210	Functional Description
0000	Schmitt-trigger test mode 2 (BP40 → BP41)
0001	Schmitt-trigger test mode 1 (BP41 or TIM1 → BP40)
0010	Melody generation with envelope
0011	Melody generator
0100	Timer/counter, reload, toggle on, 50% duty cycle
0101	Timer/counter, free running, toggle on, 50% duty cycle
0110	Pulse density modulation (PDM)
0111	Pulse width modulation (PWM)
1000	Phase shift measurement
1001	Position measurement
1010	Low pulse width measurement of BP41
1011	High pulse width measurement of BP41
1100	Timer/counter, reload, toggle off
1101	Timer/counter, free running, toggle off
1110	Period measurement, rising edge of BP41
1111	Period measurement, falling edge of BP41

3.3.1 Timer 0 Free Running Counter Modes (Strobe and 50% Duty Cycle)

In the free running counter mode, the Timer 0 can be used as an event counter for summing external event pulses on BP40 or as a timer with an internal time base clock. When enabled, the counter will count up, generating an output signal on BP41 whenever the counter contents match the compare register (see figure 19). This signal can, depending on the timer mode, appear either as a strobe pulse or as a simple toggling of the output state (50% duty cycle). Interrupts (if not masked) are generated every 256 clocks on the overflow condition. By reading the capture register, the current counter state can be read at any time. The compare register has no effect on the counter cycle time and will not influence interrupts.

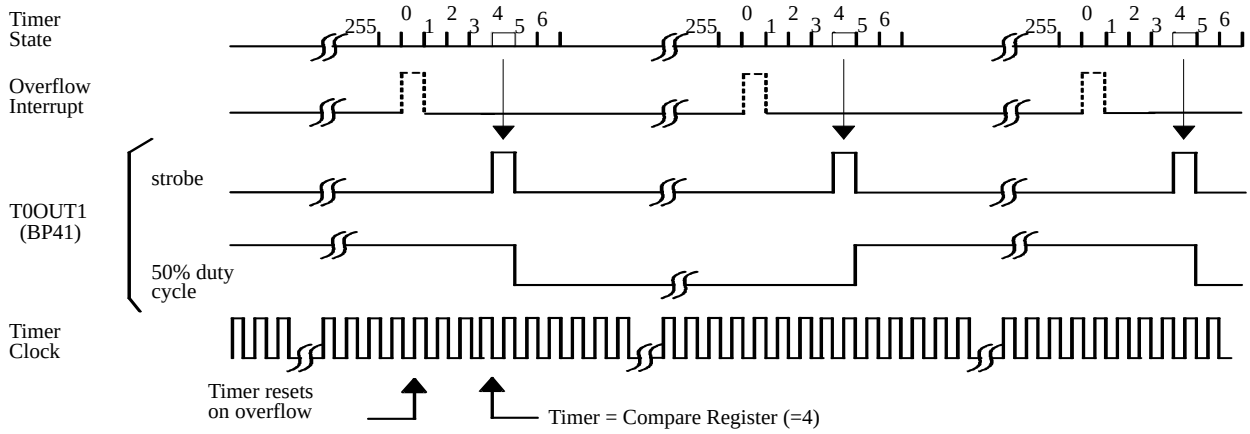


Figure 19. Timer 0 free running counter mode

3.3.2 Timer 0 Counter Reload Modes (Strobe and 50% Duty Cycle)

As in the free running mode, the counter can also be clocked from either an external signal on BP40 or from an internal clock source. In this mode, the counter repetition period is completely defined by the contents of the compare register (T0CP) (see figure 20). The counter counts up with the selected clock frequency. When it reaches the value held in the compare register, it causes the counter to return to the zero state. At the same time, depending on the selected timer mode, the BP41 either toggles or generates a strobe pulse. If the Timer 0 interrupt is unmasked, a compare interrupt is also generated.

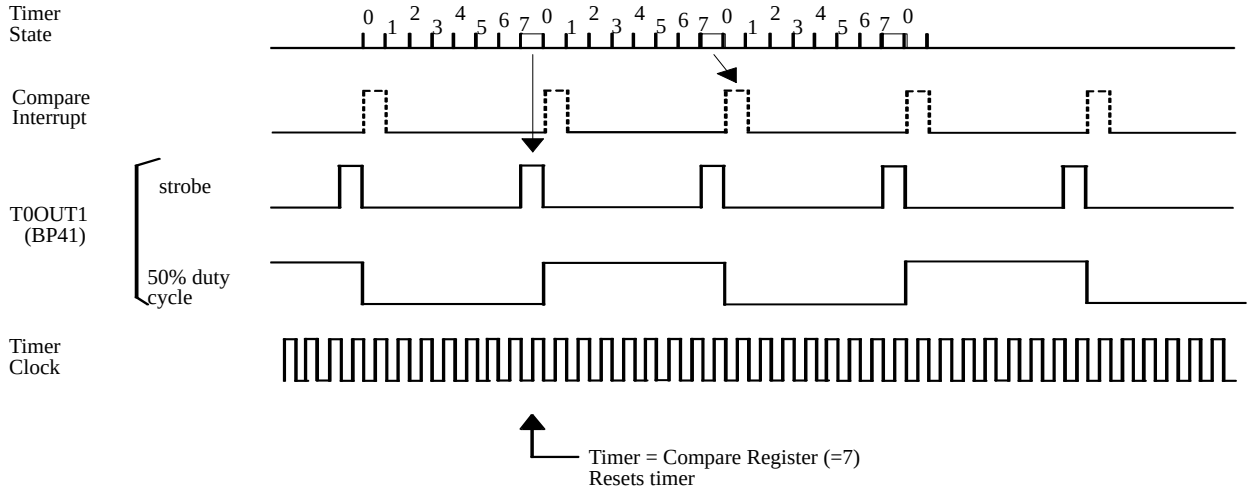
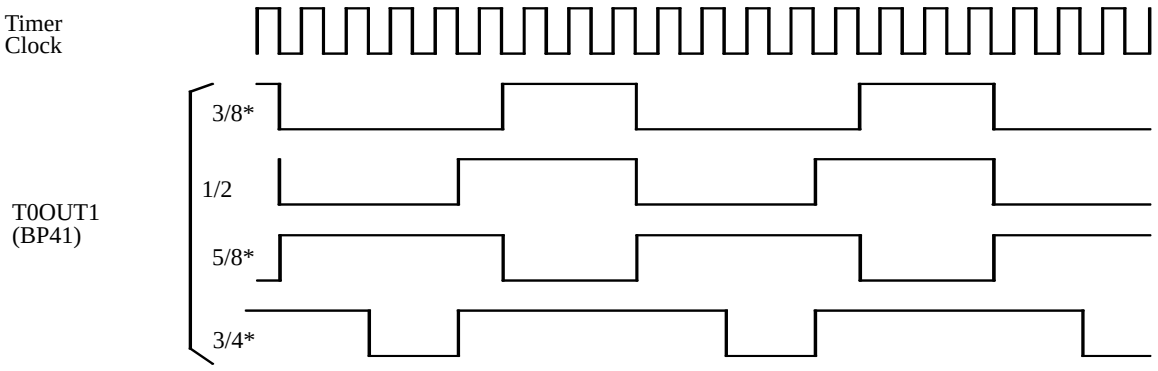


Figure 20. Timer 0 counter reload mode

Motor Chopping and Mask Options

In the counter auto reload mode (50% duty cycle), mask options are available for generating a 1 kHz or 2 kHz frequency with a duty cycles of 1/2, 3/8, 5/8 and 3/4. The resultant waveform is used as the chopping frequency for so called “motor chopping”. This technique allows the use of low cost, low voltage clock motors in applications where only higher supply voltages are available. The resultant voltage waveforms are shown in figure 21. To obtain the required motor driver waveforms on BP40 and BP41 as shown in figure 22, the user program must modulate the Timer 0 chopping frequency. This is performed by preloading Port 4 data latches (P4DAT0 and P4DAT1) with ’0’, setting the normal Port 4 direction register bits to output mode (P4DDR0 = P4DDR1 = ’0’) and switching the P4IO0 and P4IO1 register bits alternately to ’0’, on every chopping burst. The timer chopping signals are thus transferred to the port outputs. In the intermediate periods, between bursts, both P4IO0 and P4IO1 are set to ’1’ and the preloaded Port 4 data latch outputs appear on the BP40 and BP41 outputs.



* = Mask option
Timer 0 configuration: Reload mode, 50% duty cycle
Comparator value = ’F’ hex (1 kHz) or ’7’ hex (2 kHz)
Timer clock = 32 kHz (prescaler bypassed)

Figure 21. Motor chopping waveforms

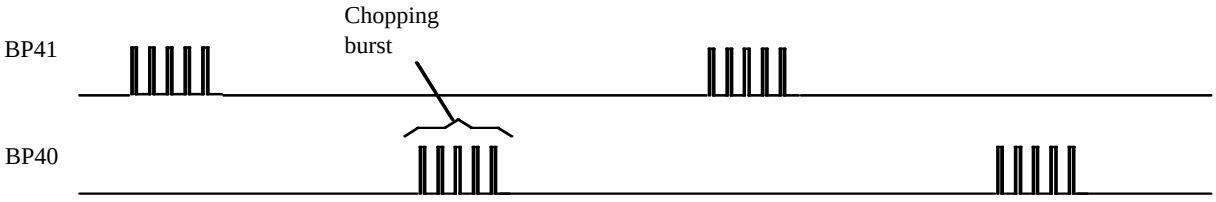


Figure 22. Motor driver output waveforms

3.3.3 Melody Mode (with/without Modulation)

The non modulated melody mode is identical to the auto-reload counter (50% duty cycle) mode. The melody tone frequency appearing on BP41 and/or BP40 is determined in exactly the same way by the value written into the comparator register.

In the modulated melody mode, the M44C636 generates two output signals, a melody tone and an envelope pulse (see figure 23). The tone frequency output on BP41 is generated in exactly the same way as in the simple melody mode. While the envelope pulse on BP40 is a single pulse, of a clock period in duration which appears shortly after loading the compare value into the compare register. In this mode, an analogue switch is activated between the BP40 and BP41 outputs (see figure 24). With the external capacitor connected, the resultant signal on BP41 exhibits a melody chime effect with an exponential decay.

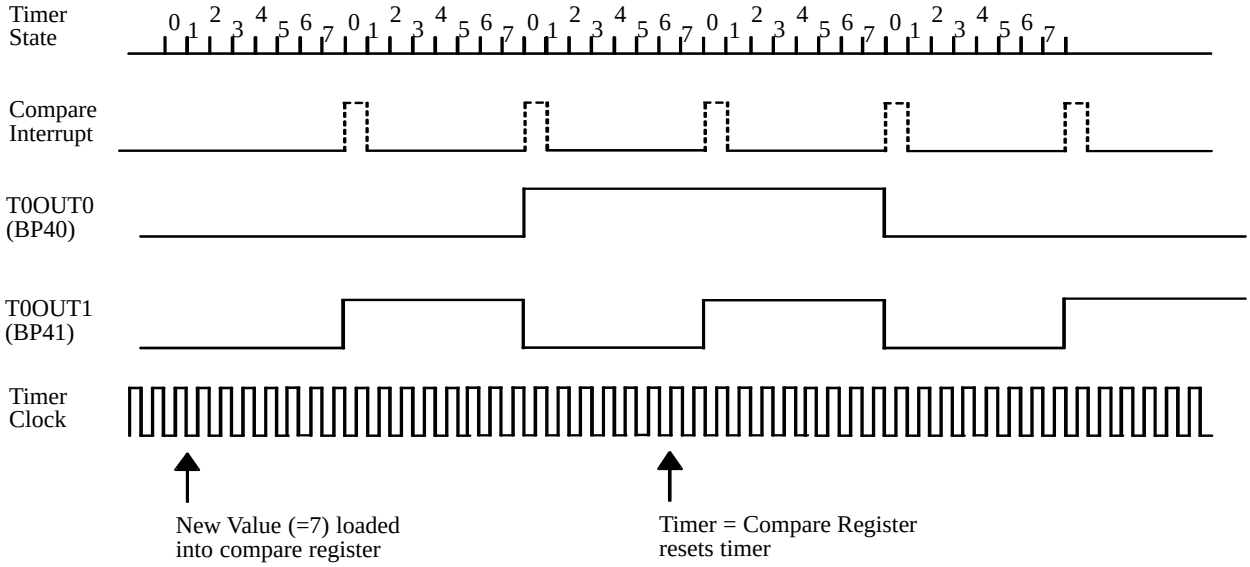


Figure 23. Modulated melody mode

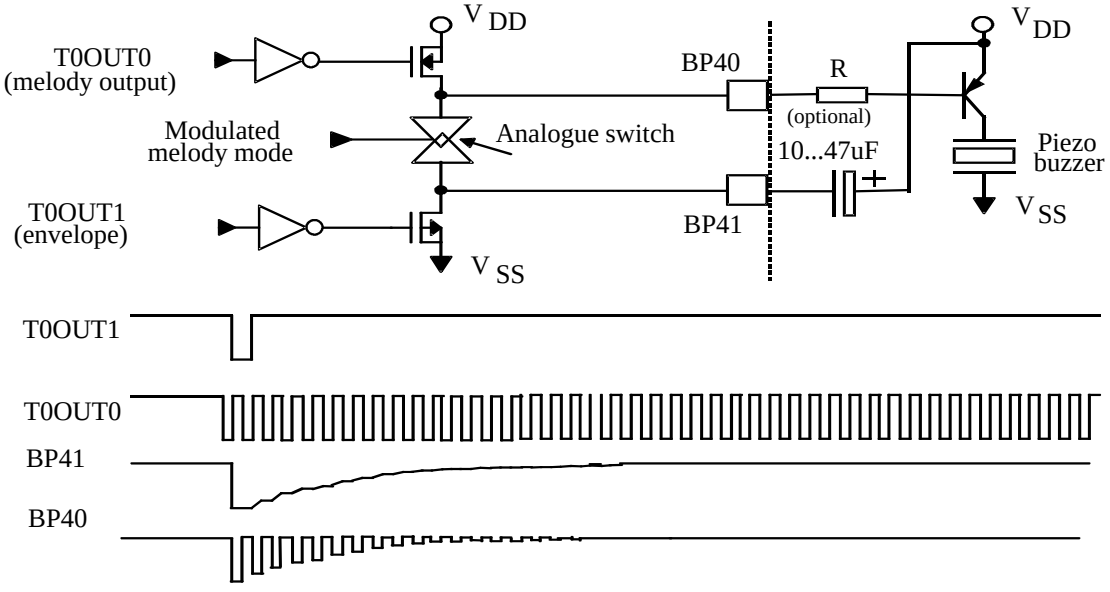
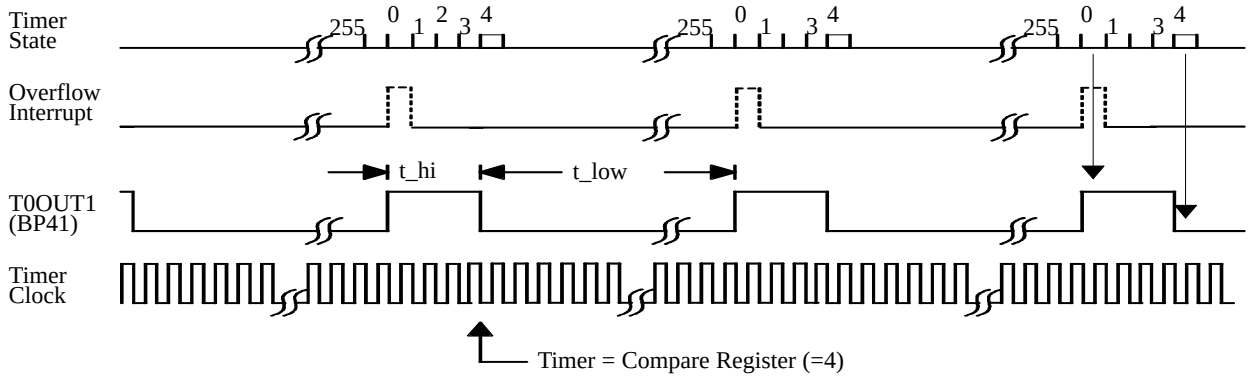


Figure 24. Modulated melody output circuit

3.3.4 Timer 0 Pulse Width Modulation Mode

A pulse width modulated (PWM) signal exhibits a fixed repetition frequency and a variable mark space ratio. It is often used as a simple method for D/A conversion, the high period is proportional to the digital value to be converted. Thus by connecting a simple low pass RC network on the PWM signal, the DC analogue value can be extracted.

The Timer 0 generates the PWM signal by comparing the state of the free running up counter with the contents of the compare register (see figure 25). If it is less, then the BP41 output is high and if it is greater or equal, then it is set low. Thus, the high phase of the PWM signal is directly proportional to the compare register contents. A total of 256 possible discrete mark space ratios can be generated ranging from a continuous low signal over a variable pulse width signal to a continuous high signal. The PWM signal has a repetition period of 256 clock periods, an interrupt (if unmasked) being generated on every overflow event. Care should be taken if the system clock frequency is used as the PWM clock source because it will stop if the CPU goes into SLEEP.



t_hi = (comparator value)*clock period
t_low = (255–comparator value)*clock period

Figure 25. Timer 0 pulse width modulation

3.3.5 Pulse Density Modulation Mode

Pulse density modulation (PDM) is also used for simple D/A conversion. Unlike the PWM signal,where the high and low signal phases are always continuous during a single repetition cycle, the PDM distributes these evenly as a series of pulses (see figure 26). This has the advantage that, if used together with an RC smoothing filter for D/A conversion, either the ripple is less than the PWM, or, for a corresponding ripple error, the filter components can be smaller or the clock frequency lower. To generate the PDM output on BP41, the pulse density is controlled by the contents of the compare register in the same way as the PWM generation. Each of the pulses has a width equal to the counter clock period.

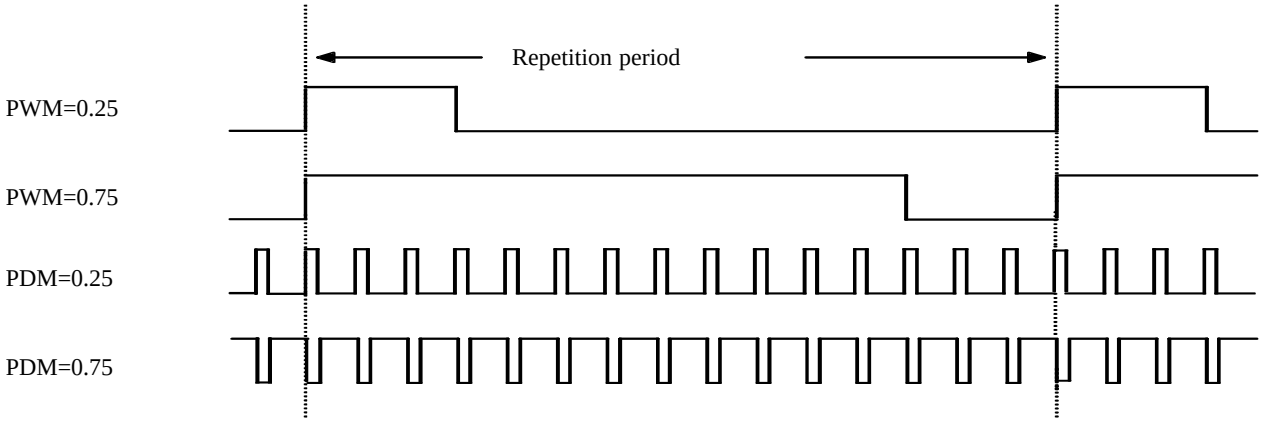


Figure 26. An example 4-bit PWM/PDM comparison

3.3.6 Phase Measurement Mode

This mode allows the Timer 0 to measure the phase misalignment between two 1:1 mark space ratio input signals connected to the BP40 and BP41 pins (see figure 27). The counter clock is gated with the phase misalignment period (tp), during which time the counter increments with the selected clock frequency. This misalignment period is defined as the period during which BP40 is high and BP41 is low. Capturing and resetting of the counter always takes place on the rising edge of BP41. The measured value remains in the capture register until overwritten by the next measurement. Interrupts can be generated by either an overflow condition or an end-of-measurement (’eom’) event. An ’eom’ event signals the CPU that a new measurement value is present in the capture register to be read, if required.

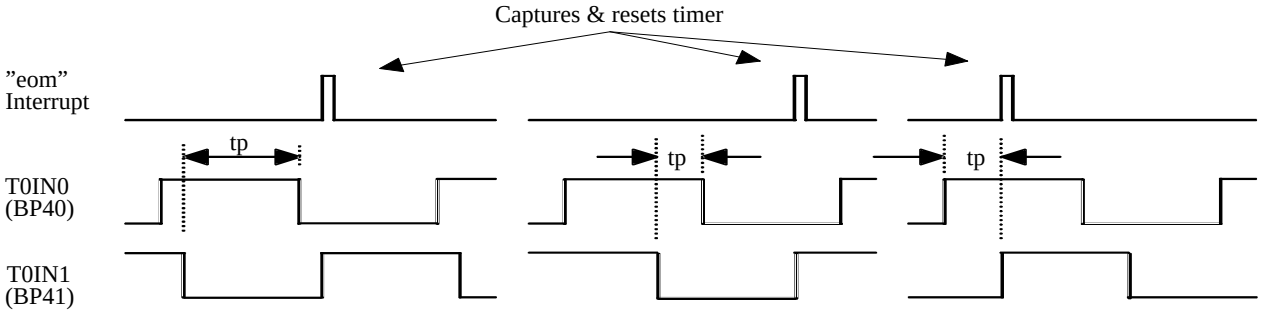


Figure 27. Phase measurement

3.3.7 Position Measurement Mode

This mode is intended for the evaluation of positional sensors with biphase output signals. Figure 28 illustrates a typical positional sensor system which delivers both incremental positional stepping signals and also directional information. The direction can be deduced from the relative phase of the two signals, so that if BP40 is high on the rising edge BP41, then the moving mask is travelling to the left and if it is low then it is travelling right. The direction (left/right) information is used to set the direction of the up/down counter with which the BP40 pulses are counted. So assuming that the system has been reset on a reference position, the counter will always hold the absolute current position of the moving mask. This can be read by the CPU when required. This mode is the only one in which the counter is allowed to decrement. So, in this case it is possible for both an underflow or an overflow to occur. The overflow interrupt (if unmasked) will trigger on either of these conditions while the compare interrupt on the other hand will only trigger if the counter is counting upwards. To differentiate between an overflow or underflow, the compare value can be set to ’0’hex for example.

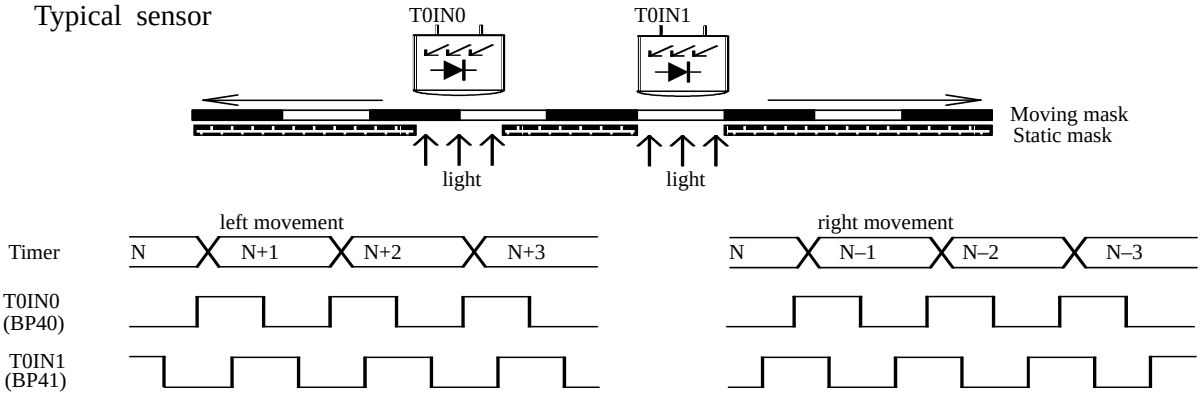


Figure 28. Position measurement mode

3.3.8 Period Measurement Modes (Rising and Falling Edge)

During the period measurement mode, the counter counts the number of either internal or external clocks in one period of the BP41 input signal (see figure 29). Dependent on the mode chosen, this will be from rising edge to the next rising edge or conversely, falling edge to the following falling edge. On the trigger edge, the counter state will be loaded into the capture register and subsequently reset. The measurement value remains in the capture register until overwritten by the following measurement value. Interrupts can be generated by either an overflow condition or an end-of-measurement (eom) event. An eom event signals the CPU that a new measurement value is present in the capture register to be read if required.

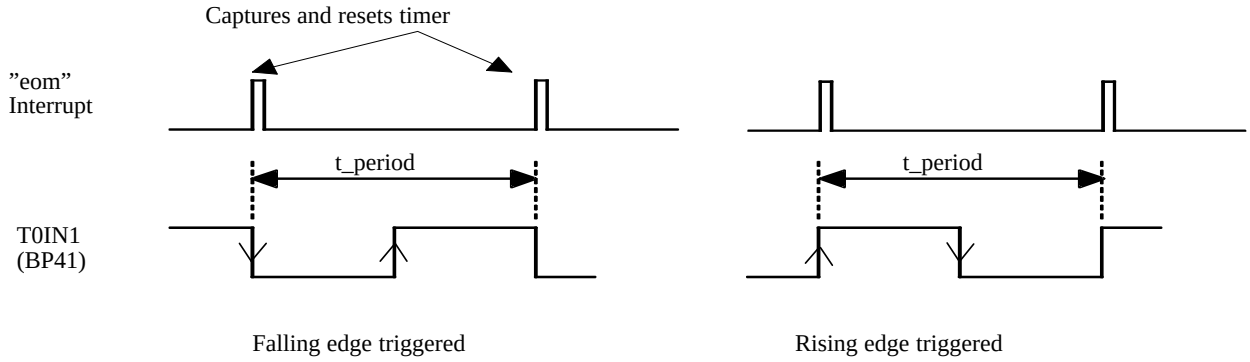


Figure 29. Period measurement

Timer 0 Control Register (T0CR)

Subport address ’1’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T0CR	**T0FS3**	**T0FS2**	**T0FS1**	**T0IM**	**Reset value: 1111b**

T0FS3 ... 1 – Timer 0 input frequency select

T0IM – Timer 0 Interrupt Mask

The timer/counter is running with an input frequency selected by the Timer 0 control register T0CR (see table 9), or is clocked by an external pulse train available at BP41.

Table 9. Timer 0 control register T0CR

3210	Functional Description
XXX0	Timer 0 interrupt enable (priority level 4)
XXX1	Timer 0 interrupt disable (priority level 4)
	Input frequency select
000X	f_C = 32,768 Hz
001X	2,048 Hz
010X	1,024 Hz
011X	512 Hz
100X	256 Hz
101X	128 Hz
110X	VALIDATE (system clock frequency)
111X	External source at BP41

Timer 0 Compare Register (T0CP) – Byte Write

The compare registers **T0CP** is 8-bit wide and must be accessed as byte wide subports (see section “Timer/Counter I/O Addressing”). They are written low nibble first followed by the high nibble. Any timer interrupt is automatically suppressed until the complete compare value has been transferred.

Subport address (write access): ’9’hex

		Bit 3	Bit 2	Bit 1	Bit 0	
T0CP	**First write cycle**	**T0CP3**	**T0CP2**	**T0CP1**	**T0CP0**	**Reset value: xxxxb**
		Bit 7	Bit 6	Bit 5	Bit 4	
	Second write cycle	**T0CP7**	**T0CP6**	**T0CP5**	**T0CP4**	**Reset value: xxxxb**

T0CP3 ... T0CP0 – Timer 0 Compare Register Data (low nibble) – first write cycle

T0CP7 ... T0CP4 – Timer 0 Compare Register Data (high nibble) – second write cycle

Timer 0 Capture Register (T0CA) – Byte Read

The 8-bit capture register **T0CA** is read as a byte wide subport. Note however, unlike the writing to the compare register, the high nibble is read first followed by the low nibble. The 8-bit timer state is captured on reading the first nibble and held until the complete byte has been read. During this transfer the timer is free to continue counting.

Subport address (read access): ’9’hex

		Bit 7	Bit 6	Bit 5	Bit 4	
T0CA	**First read cycle**	**T0CA7**	**T0CA6**	**T0CA5**	**T0CA4**	**Reset value: 0000b**
		Bit 3	Bit 2	Bit 1	Bit 0	
	Second read cycle	**T0CA3**	**T0CA2**	**T0CA1**	**T0CA0**	**Reset value: 0000b**

T0CA7. .. T0CA4 – Timer 0 Capture Register Data (high nibble) – first read cycle

T0CA3 ... T0CA0 – Timer 0 Capture Register Data (low nibble) – second read cycle

3.4 Timer 1 Modes

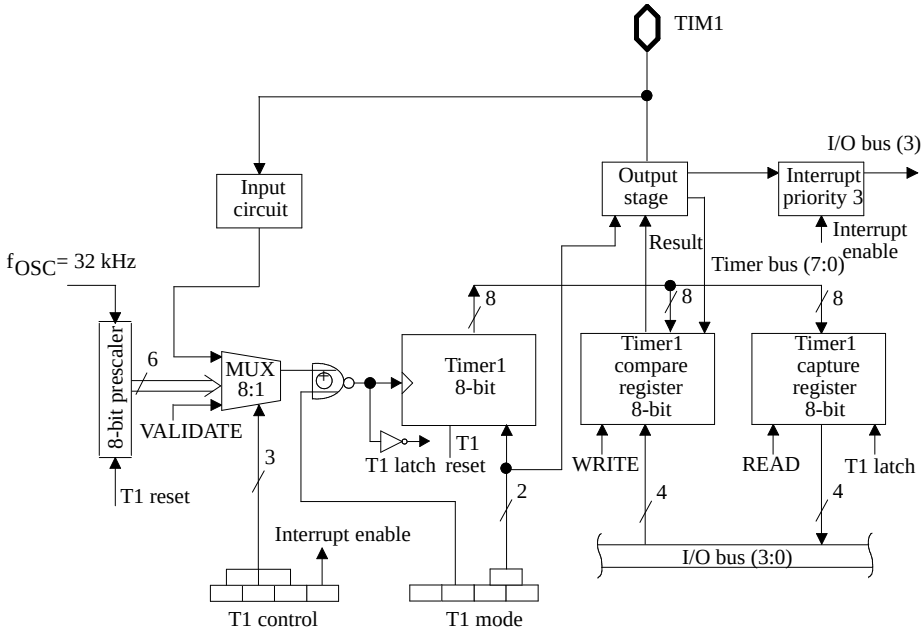


Figure 30. Block diagram of Timer 1

Timer 1 is an asynchronous up-counter. Depending on the programmed timer/counter mode an interrupt of priority level 3 is generated on a successful compare of the Timer 1 count value and the Timer 1 compare register. The Timer 1 I/O pin is named **TIM1** and its direction is automatically controlled by the hardware.

The four different operating modes of Timer 1 are programmed with the Timer 1 mode register T1MO. The active edge is programmable by bit 2 of the mode register. Refer to the following paragraphs for more detailed information about the modes shown in table 10.

Refer to the following paragraphs for more information about the Timer 1 modes listed in table 10.

Timer 1 Mode Register (T1MO)

Subport address: ’2’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T1MO	**T1MO3**	**T1MO2**	**T1MO1**	**T1MO0**	**Reset value: 1111b**

T1MO3 ... 0 Timer 1 Mode Code

Table 10. Timer 1 mode register T1MO

3210	Functional Description
1X00	Timer/counter, free running, toggle off
1X01	Timer/counter, reload, toggle on
1X10	Pulse width modulation (PWM)
1X11	Timer/counter, reload, toggle off
X0XX	Count on falling edge
X1XX	Count on rising edge
0XXX	Timer 1 Schmitt-trigger test mode (TIM1 → BP40)

Timer 1 Control Register (T1CR)

Subport address ’3’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T1CR	**T1FS3**	**T1FS2**	**T1FS1**	**T1IM**	**Reset value: 1110b**

T1FS3 ... 1 – Timer 1 input frequency select

T1IM – Timer 1 Interrupt Mask

The timer/counter is running with an input frequency selected by the Timer 1 control register T1CR (see table 11) or is clocked by an external pulse train available at the TIM1 pin. If enabled, an interrupt is generated at any timer/counter compare value match.

Table 11. Timer 1 control register T1CR

3210	Functional Description
XXX0	Timer 1 interrupt enable (priority level 3)
XXX1	Timer 1 interrupt disable (priority level 3)
	Input frequency select
000X	f_C = 32,768 Hz
001X	8,192 Hz
010X	1,024 Hz
011X	512 Hz
100X	256 Hz
101X	128 Hz
110X	VALIDATE (system clock frequency)
111X	External source at TIM1

3.4.1 Timer 1 Free Running Counter Mode

In the free running counter mode, the Timer 1 can be used as an event counter for summing external event pulses on **TIM1** or as a timer with an internal time base clock. When enabled, the counter will count up, generating an interrupt (if not masked) every 256 clocks whenever the counter contents match the programmed **T1CP** compare register value. By reading the capture register **T1CA**, the current counter state can be read at any time.

3.4.2 Timer 1 Counter Reload Mode (Toggle On/Off)

This operating mode is similar to the free running mode except that the timer/counter restarts automatically from zero on each successful match with the **T1CP** compare register value. If ’toggle on’ is selected a resulting output frequency of (50% duty cycle) of

$$f_{OUT} = \frac{f_{IN}}{2 * (n + 1)}$$

with n = 1 to 255 can be observed at **TIM1**. See figure for the corresponding timing waveforms visible at **TIM1**.

3.4.3 Timer 1 Width Modulation Mode

The Timer 1 generates the PWM signal by comparing the state of the free running up-counter with the contents of the Timer 1 compare register **T1CP**. Provided that the contents of this register is greater than the counter value, the **TIM1** output is set LOW, if the contents of this register is less or equal to the counter value, the output will be HIGH. The pulse width ratio is therefore, defined by the contents of the compare register, in the range of 0 to 1 and may be programmed in increments of 1/255 (see figure 25). If enabled, an interrupt is generated on each match with the compare value. This interrupt should be used to write a new value into the compare register. During this mode of operation, where the processor’s system clock (VALIDATE) is used as input frequency to the counter, care must be taken that the processor is kept in active mode.

Timer 1 Compare Register (T1CP) – Byte Write

The compare registers **T1CP** is 8-bit wide and must be accessed as byte wide subports (see section “Timer/Counter I/O Addressing”). They are written low nibble first followed by the high nibble. Any timer interrupt is automatically suppressed until the complete compare value has been transferred.

Subport address (write access): ’8’hex

		Bit 3	Bit 2	Bit 1	Bit 0	
T1CP	**First write cycle**	**T1CP3**	**T1CP2**	**T1CP1**	**T1CP0**	**Reset value: xxxxb**
		Bit 7	Bit 6	Bit 5	Bit 4	
	Second write cycle	**T1CP7**	**T1CP6**	**T1CP5**	**T1CP4**	**Reset value: xxxxb**

T1CP3 ... T1CP0 – Timer 1 Compare Register Data (low nibble) – first write cycle

T1CP7 ... T1CP4 – Timer 1 Compare Register Data (high nibble) – second write cycle

Timer 1 Capture Register (T1CA) – Byte Read

The 8-bit capture register **T1CA** is read as a byte wide subport. Note however, unlike the writing to the compare register, the high nibble is read first followed by the low nibble. The 8-bit timer state is captured on reading the first nibble and held until the complete byte has been read. During this transfer the timer is free to continue counting.

Subport address (read access): ’8’hex

		Bit 7	Bit 6	Bit 5	Bit 4	
T1CA	**First read cycle**	**T1CA7**	**T1CA6**	**T1CA5**	**T1CA4**	**Reset value: 0000b**
		Bit 3	Bit 2	Bit 1	Bit 0	
	Second read cycle	**T1CA3**	**T1CA2**	**T1CA1**	**T1CA0**	**Reset value: 0000b**

T1CA7. .. T1CA4 – Timer 1 Capture Register Data (high nibble) – first read cycle

T1CA3 ... T1CA0 – Timer 1 Capture Register Data (low nibble) – second read cycle

Timer/Counter Mode Register (TCMO)

Subport address: ’4’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
TCMO	not used	**TC8**	**T1RST**	**T0RST**	**Reset value: x111b**

TC8 – Timer/Counter 8-/16-bit mode

T1RST – Timer 1 Reset/Run

T0RST – Timer 0 Reset/Run

Table 12. Timer/counter mode register TCMO

3210	Functional Description
XXX0	Timer 0 running
XXX1	Timer 0 reset
XX0X	Timer 1 running
XX1X	Timer 1 reset
X0XX	16-bit mode
X1XX	8-bit mode

3.5 16-bit Timer/Counter Mode

In this mode Timer 1 is clocked by the interrupt signal of Timer 0 even if the Timer 0 interrupt is disabled. Timer 0 and Timer 1 can be programmed individually, so care must be taken to ensure that the 16-bit mode is set correctly. BP40, BP41 and **TIM1** work as in the 8-bit timer modes. The Timer 1 control register **T1CR** has no function in this mode.

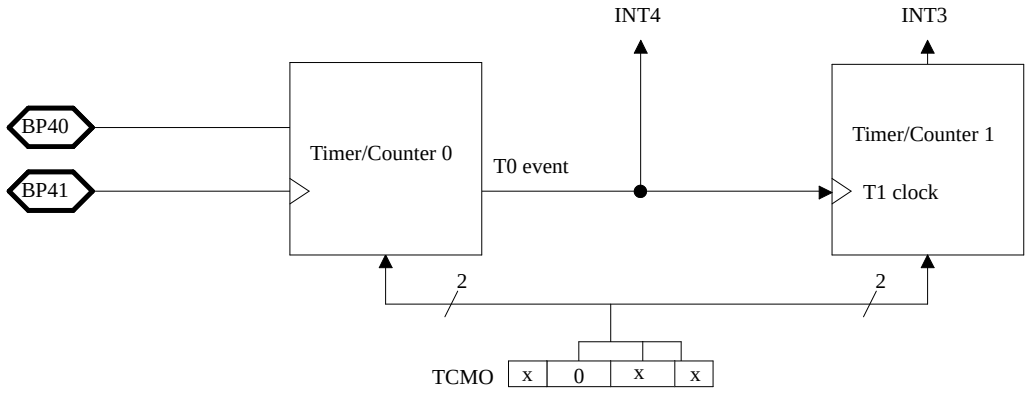


Figure 31. Timer/counter 16-bit mode

Port 4 I/O Control Register (P4IOR)

Subport address: ’5’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
P4IOR	**P4IOR3**	**P4IOR2**	**P4IOR1**	**P4IOR0**	**Reset value: 1111b**

Table 13. Timer 0 and Port 4 I/O control register P4IOR

3210	Functional Description
XXX0	BP40 is Timer 0 I/O pad
XXX1	BP40 is Port 4 pad
XX0X	BP41 is Timer 0 I/O pad
XX1X	BP41 is Port 4 pad
X0XX	BP42 frequency output (8 kHz or 32 kHz mask option)
X1XX	BP42 is Port 4 pad
0XXX	Port 4 data direction register is enabled (bitwise I/O)
1XXX	Port 4 works in nibble-wise I/O mode (as Port 0/1)

3.5.1 Port 4 Data Direction Register (P4DDR)

Subport address: ’6’hex

	Bit 3	Bit 2	Bit 1	Bit 0	
PxDDR	**P4DDR3**	**P4DDR2**	**P4DDR1**	**P4DDR0**	**Reset value: 1111b**

Value: 1111b means all pins in input mode

Table 14. Port 4 data direction control register P4DDR

3210	Functional Description
XXX0	BP40 is input
XXX1	BP40 is output
XX0X	BP41 is input
XX1X	BP41 is output
X0XX	BP42 is input
X1XX	BP42 is output
0XXX	BP43 is input
1XXX	BP43 is output

Timer 0 Capture Register (T0CA) – Byte Read

Subport address (read access): ’9’hex

		Bit 7	Bit 6	Bit 5	Bit 4	
T0CA	**First read cycle**	**T0CA7**	**T0CA6**	**T0CA5**	**T0CA4**	**Reset value: 0000b**
		Bit 3	Bit 2	Bit 1	Bit 0	
	Second write cycle	**T0CA3**	**T0CA2**	**T0CA1**	**T0CA0**	**Reset value: 0000b**

4 Liquid Crystal Display Driver

This chapter describes the programming of the LCD driver. It also includes

- Information about the relationship between a typical 7 segment numeric display, the segment and backplane outputs (for 2:1, 3:1, and 4:1 multiplex)
- Waveform examples for the different LCD drive modes

Figure 32 is a functional block diagram of the LCD driver circuitry. The internal I/O bus is connected to the LCD control register (Port 2) and the LCD data register (Port 3). The LCD driver interface to the programmer comprises these two output ports.

The LCD driver circuitry offers the following features:

- Drives up to 80 display segments
- Supports 3 V LCD panels over the full supply voltage range
- Built-in LCD voltage generation with temperature compensation
- Current consumption of LCD voltage generation adaptable to display size
- Display continues when µC in SLEEP mode
- Programmable multiplex rate: direct drive, 2:1, 3:1 or 4:1 multiplex mode.

4.1 Display Data Register

The LCD data register receives the data from the µC and processes it in a 4-bit wide circular 20 stage shift register. The functional block diagram (figure 32) shows the order of the segment information and the way it has to be written into the shift register (starting with the 20th segment).

A logic 1 in the shift register's bit-map indicates the ON state of the corresponding LCD segment. Similarly a logic 0 indicates the OFF state. There is a 1:1 correspondence between each stage of the shift register and the segment outputs, and between the individual bits of a register nibble and the backplane outputs. The LSB of each nibble corresponds to the 20 segments operated with respect to backplane **COM0**. In multiplexed LCD applications the segment data of the second, third and fourth column of the shift register are time multiplexed with **COM1**, **COM2** and **COM3** respectively. The LCD specific segment decoding is done via qFORTH software routines, thus omitting the need for separate decoding circuitry.

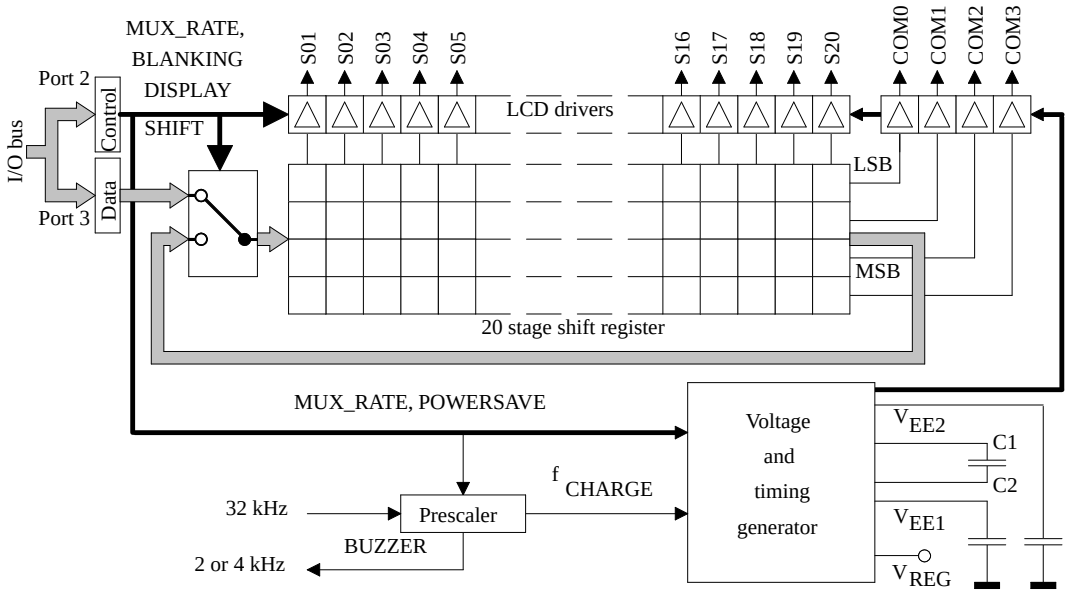


Figure 32. LCD driver – functional block diagram

4.2 LCD Control Register

Table 15. LCD driver – operation mode programming

Control Mode	Operation Mode
0	DRIVE DIRECT
1	2:1 MULTIPLEX
2	3:1 MULTIPLEX
3	DISPLAY the current LCD data register contents
4	CLEAR/INITIALIZE and set up of 4:1 MULTIPLEX mode
5	Circular SHIFT current LCD data register contents by 1 segment
6	BLANKING of all segments
7	POWERSAVE will switch off all LCD voltages
15	TOGGLE_BUZZER output frequency (2 kHz ⇐⇒ 4 kHz)

The LCD control register receives the operation mode data at port2 to configure the LCD driver circuitry (refer to table 15).

4.2.1 Initializing the LCD Driver

After power-on the LCD driver circuitry is set automatically into BLANKING and 4:1 multiplex drive mode. After any reset condition, a proper operation of the LCD driver is ensured by writing the following control codes into the LCD control register:

- CLEAR/INITIALIZE
- Multiplex drive mode, if not 4:1 multiplex.

Four terms can be used to set the multiplex rate (refer to table 15). The CLEAR/INIT term initializes the LCD driver, setting it into the 4:1 multiplex drive mode. Therefore no extra control code is needed for 4:1 multiplex. After any hardware reset, the contents of the LCD display data registers are undefined and should be initialized with the following instruction sequence:

- Write BLANKING to the LCD control register (optionally)
- Write 20 times 'Fh' to the LCD data register. This is an useful production test to check that all LCD segments are available and connected
- Write DISPLAY to the LCD control register
- Set up charge pumping frequency for the LCD voltage generator, if display is small.

4.2.2 LCD Driver Modes of Operation

In normal timekeeping applications the DISPLAY command might be given only once at the end of the first complete LCD display update (e.g. "Mo 12:00"). Afterwards a total display change consists of up to 20 consecutive nibbles written to the LCD data register.

The BLANKING term causes a blank display and might be necessary before each new data transfer to the display registers. This is especially true when the µC is heavily loaded by a number of interrupt sources and the LCD update is handled as a base task. Whilst the processor is writing to the LCD data register, the data in the addressed latch is also being read by the scan logic circuitry. The BLANKING will be removed at the end of the data transfer by writing DISPLAY. If the DISPLAY command is not given, the BLANKING remains which allows the easy implementation of a blinking display.

When using the SHIFT term, only nibbles requiring an update need to be software decoded and written to the LCD data register. The data to be retained is simply shifted back to its original position, whilst new data nibbles are inserted in the appropriate position (refer to figure 32).

As an example for the effective use of the SHIFT term, the implementation of a 6 digit (3:1 multiplex) LCD panel test is described:

- Set up the LCD driver for 3:1 multiplex
- Switch on all segments of the leading 7 segment digit (including the attenuator, see figure 38) with a complete LCD display update
- After (half of) a second, write SHIFT to the LCD control register. Write three dummy values to the LCD data register to support the shift clock pulses. This operation will scroll the digit one position to the right
- After a total of five operations, the digit appears in the right-most position and the (BLANKING or) DISPLAY term should be given to the control register to overwrite the SHIFT multiplexer configuration.

The POWERSAVE term blanks the LCD by switching all the LCD voltage levels to V_{SS}, thus causing a reduction

in display power consumption. This mode is only effective if the display is generally to be blanked for periods of more than 5 seconds. The display information is still kept in the LCD data shift register. By writing DISPLAY into the LCD control register, the old contents will be visible again.

4.2.3 Programming of the Buzzer Frequency

After any hardware reset, power on reset or CLEAR/INITIALIZE command to the LCD controller, the buzzer output frequency is reset to 2 kHz.

To toggle the output frequency under software control, the following command sequence has to be written to the LCD control register (Port 2):

- Write the TOGGLE_BUZZER (Fh) command to the LCD control port
- Write the DISPLAY (3h) command to the LCD control port.

The first time this sequence is executed will set the buzzer frequency to 4 kHz. Each ”Clear/Init” or each second write of the frequency toggle command will reset the buzzer frequency back to 2 kHz. This feature allows the usage of use different frequencies for separate signal functions.

4.2.4 Reduction of LCD Charge Pumping Frequency

After any power-on or hardware reset, the LCD voltage generator is in the fast charge mode. This mode is used to quickly charge the capacitance of large displays by using a high charge pumping frequency for the LCD voltage generator. For smaller displays and to reduce the overall system current the M44C636 allows the modification of the charge frequency under software control.

With each read from the LCD control register (Port 2), the charge frequency is divided by 2. After four consecutive read operations, the LCD controller then is in the fast charge mode again. The charge frequency currently programmed can be observed at the C1 or C2 terminals.

4.3 LCD Voltage and Timing Generator

The LCD voltage generator circuitry boosts the regulated liquid crystal display voltage ($\mathbf{V_{REG}}$) to the doubled and tripled voltage components ($\mathbf{V_{EE1}}$, $\mathbf{V_{EE2}}$) required by multiplexed liquid crystal displays. These voltage levels are applied to the driver circuitry (see figure 32).

Most low voltage (3 V) LCD panels have a temperature coefficient of –6 mV/°C. The temperature compensated reference for the LCD voltage booster circuitry ($\mathbf{V_{REG}}$), has the task of meeting this requirement directly, so that the user gets the best LCD contrast over the full operating temperature and supply voltage range. The external components for the LCD voltage generation (one pump and two storage capacitors) should be connected to the µC as shown in figure 33. For very small LCD panels the capacitor values and charge pumping frequency may be reduced to save costs and system current. The capacitor values may be reduced from 100 nF to 47 nF. The user has to connect the µC and the LCD as it will be in the final product in order to select the capacitor value. To examine the LCD driver waveforms, an oscilloscope with a low capacitance probe should be used.

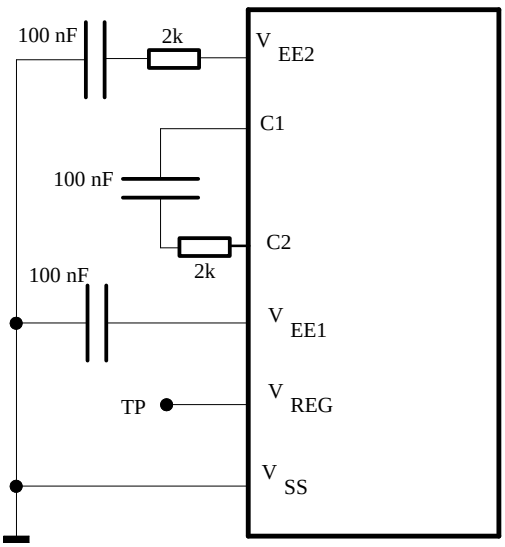


Figure 33. External components

Table 16. LCD charge frequency programming

Control Sequence	LCD Multiplex Drive Mode				DC Offset
	4:1 Multiplex		3:1, 2:1 or Direct Drive		[mV]
Default set up after POR and **NRST**	2,048	Hz	1,024	Hz	< 10 mV
1 x LCD control register read	512	Hz	512	Hz	< 10 mV
2 x LCD control register read	256	Hz	256	Hz	10 mV
3 x LCD control register read	128	Hz	128	Hz	< 50 mV
4 x LCD control register read	2,048	Hz	1,024	Hz	< 10 mV

4.4 Direct Drive Mode

The static LCD drive mode is used when a single backplane is provided at the LCD. The LSB of each stage of the display shift register directly maps to the corresponding segment driver. Sample backplane and segment drive waveforms for this mode are shown in figure 34. The following formulas are valid in the DIRECT DRIVE mode at any instant (t):

$$V_{State1}(t) = V_{S01}(t) - V_{COM0}(t)$$

$$V_{State2}(t) = V_{S02}(t) - V_{COM0}(t)$$

$$V_{ON(rms)} = V_{EE2}$$

$$V_{OFF(rms)} = \frac{V_{EE2}}{3} = V_{REG}$$

$$V \Rightarrow \text{Contrast ratio} = V_{ON(rms)}/V_{OFF(rms)} = 3$$

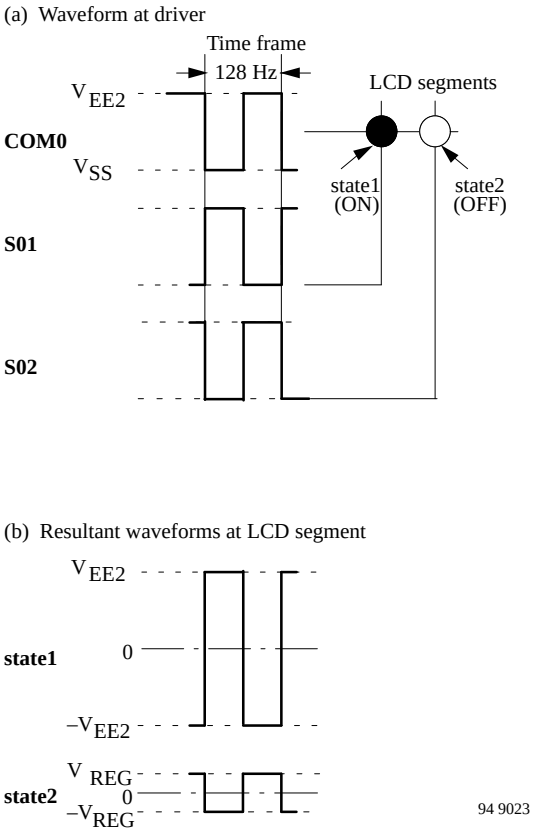


Figure 34. Direct drive mode waveforms

4.5 2:1 Multiplex Drive Mode

Figure 35 shows the connection of a 2:1 multiplex 5 digit LCD panel having the numeric display pattern shown in figure 36, the segment outputs (**S01-S20**), and the backplane outputs (**COM0, COM1**).

In the example ”456.78” is displayed on the LCD panel and the corresponding contents of the display data register is shown. Backplane and segment drive waveforms for this mode are shown in figure 37.

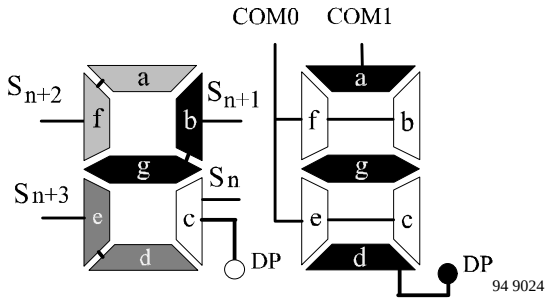


Figure 35. 2:1 multiplex 7 segment digit

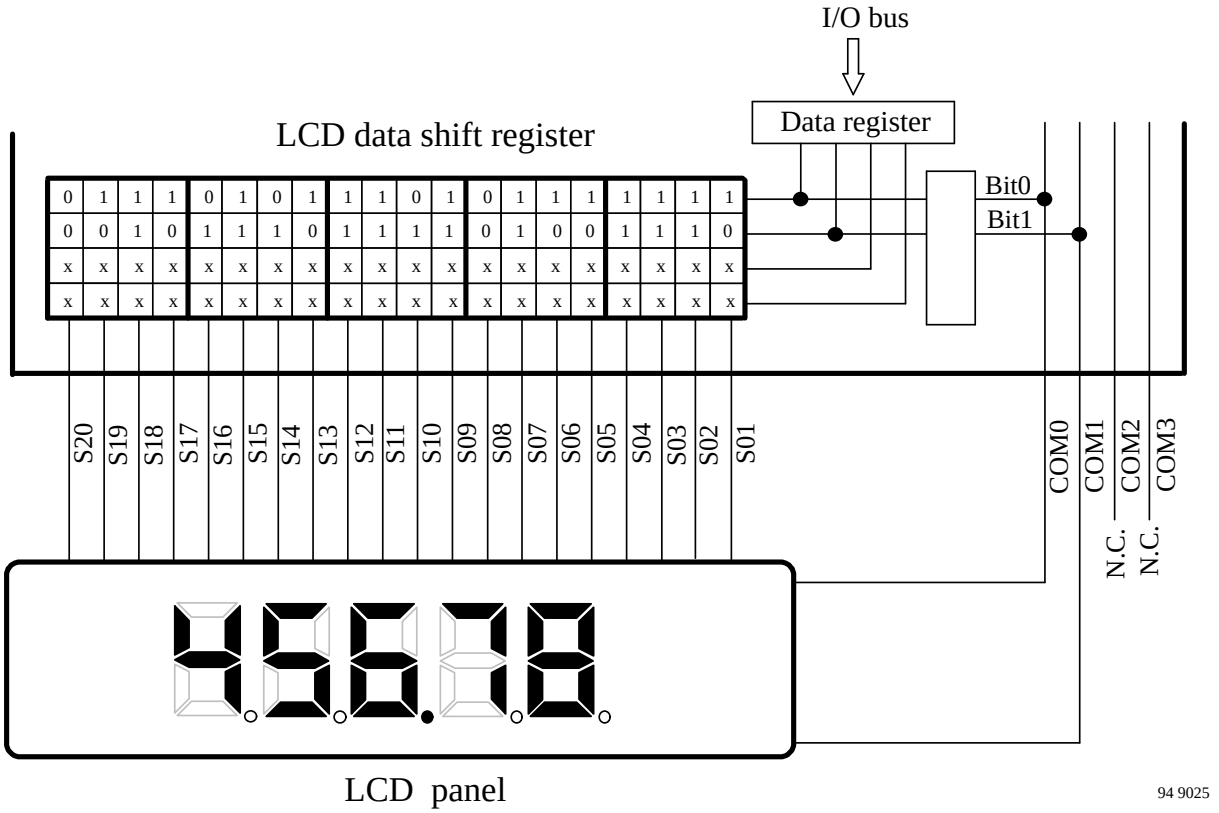
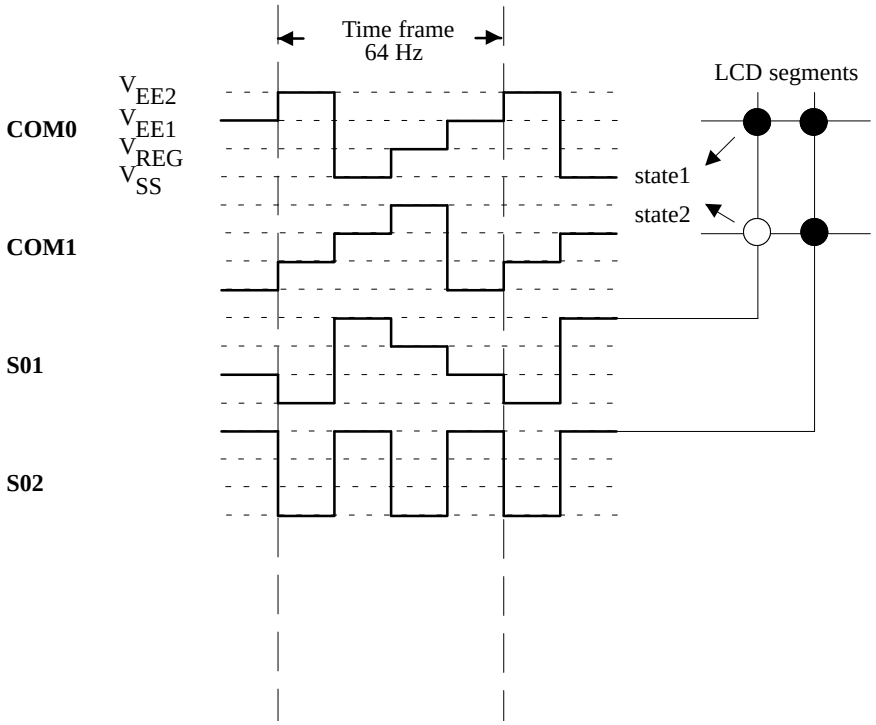


Figure 36. 2:1 multiplex LCD panel connection

(a) Waveforms at driver



(b) Resultant waveforms at LCD segment

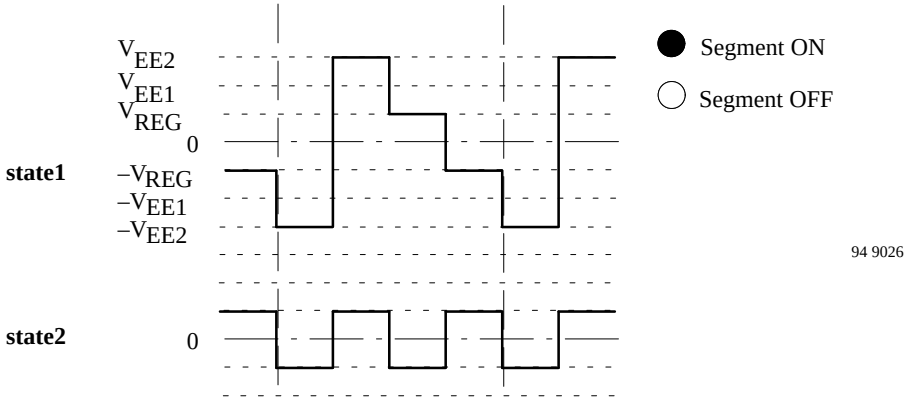


Figure 37. Waveforms for 2:1 multiplex drive mode

The following formulas are valid in the 2:1 multiplex drive mode at any instant (t):

$V_{State1}(t) = V_{S01}(t) - V_{COM0}(t)$ and $V_{State2}(t) = V_{S02}(t) - V_{COM1}(t)$

$V_{ON(rms)} = \frac{V_{EE2}}{3}\sqrt{5} = 0.745\ V_{EE2}$ and $V_{OFF(rms)} = \frac{V_{EE2}}{3}$

Contrast ratio $= V_{ON(rms)} / V_{OFF(rms)} = 2.23$

4.6 3:1 Multiplex Drive Mode

Figure 38 shows the connection of a 3:1 multiplex $6^3/_4$ digit LCD panel having the numeric display pattern shown in figure 39, the segment outputs (**S01-S20**), and the backplane outputs (**COM0-COM2**).

In the example, ”123456.7” is displayed (with a max. displayable value of ”3999999”) and the corresponding contents of the LCD display data register is shown. Backplane and segment drive waveforms for this mode are shown in figure 40.

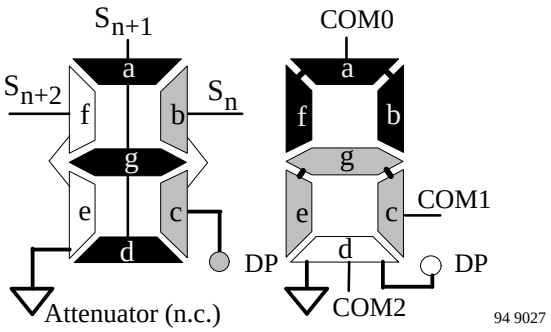


Figure 38. 3:1 multiplex 7 segment digit

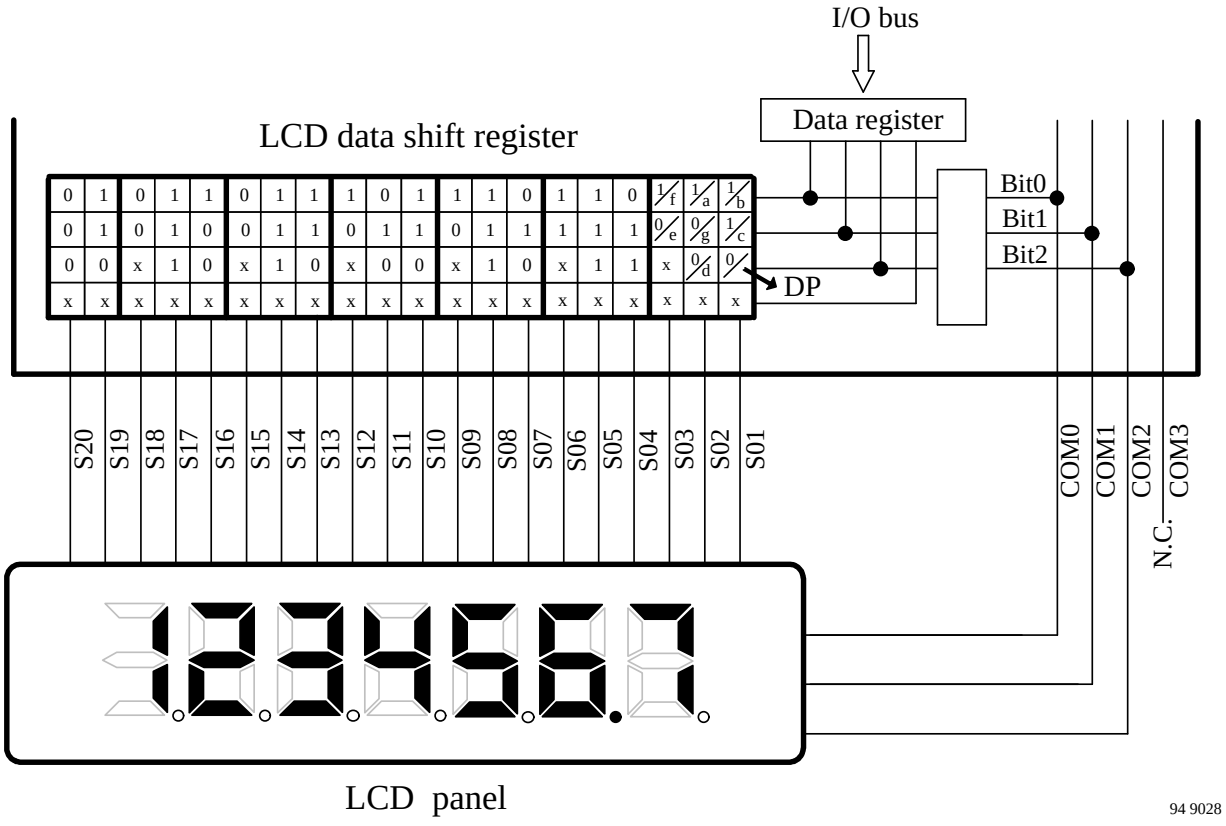


Figure 39. 3:1 multiplex LCD panel connection

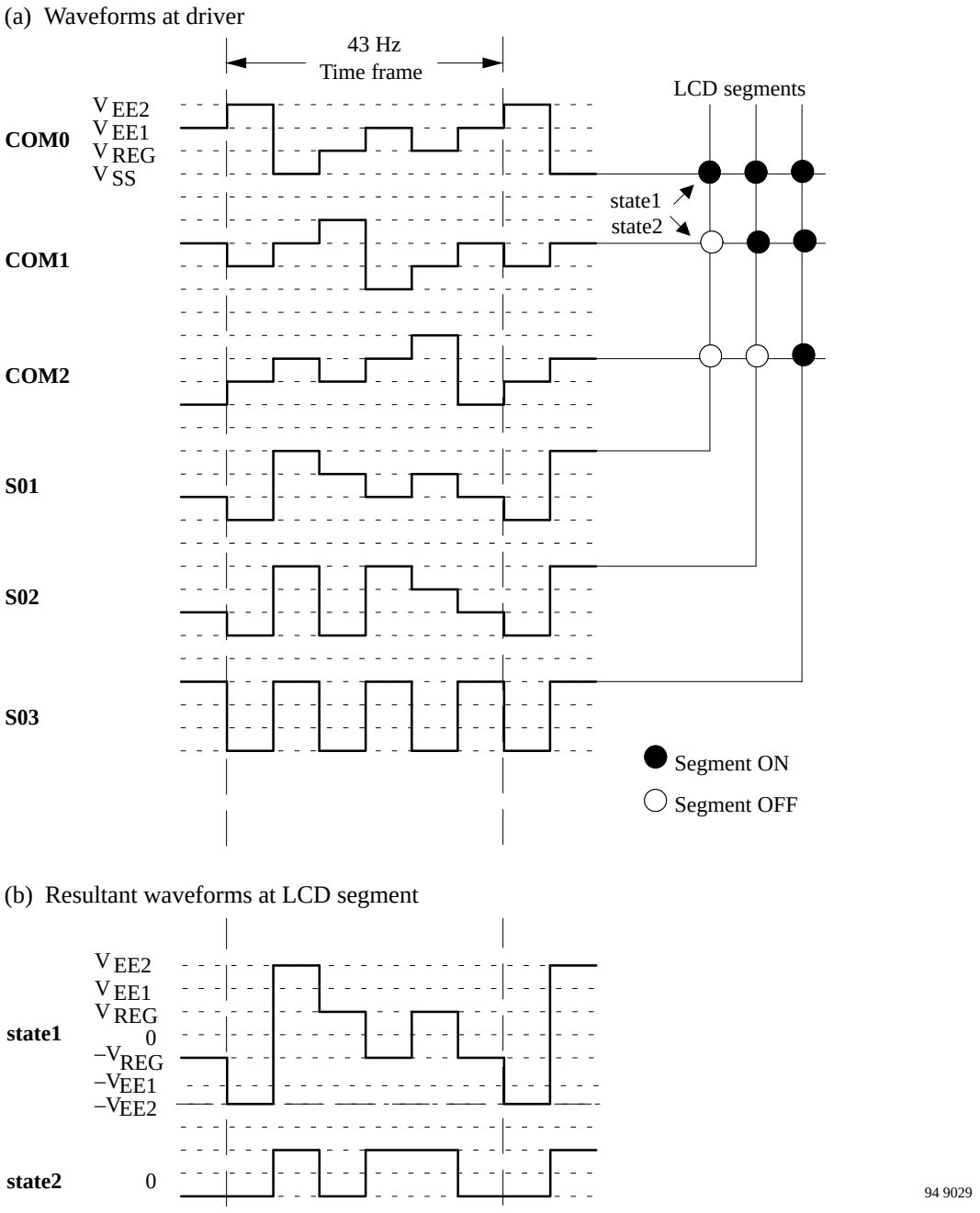


Figure 40. Waveforms for 3:1 multiplex drive mode

The following formulas are valid in the 3:1 multiplex drive mode at any instant (t):

$V_{State1}(t) = V_{S01}(t) - V_{COM0}(t)$ and $V_{State2}(t) = V_{S02}(t) - V_{COM1}(t)$

$V_{ON(rms)} = \frac{V_{EE2}}{9}\sqrt{33} = 0.638\ V_{EE2}$ and $V_{OFF(rms)} = \frac{V_{EE2}}{3}$

Contrast ratio = $V_{ON(rms)} / V_{OFF(rms)} = 1.915$

4.7 4:1 Multiplex Drive Mode

Figure 41 shows the connection of a 4:1 multiplex 10 digit LCD panel having the numeric display pattern shown in figure 42, the segment outputs (**S01-S20**), and the backplane outputs (**COM0-COM3**).

In the example, ”123456.7890” is displayed and the corresponding contents of the LCD display data register is shown. Backplane and segment drive waveforms for this mode are shown in figure 43.

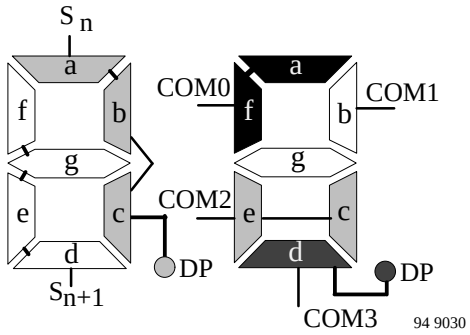


Figure 41. 4:1 multiplex 7 segment digit

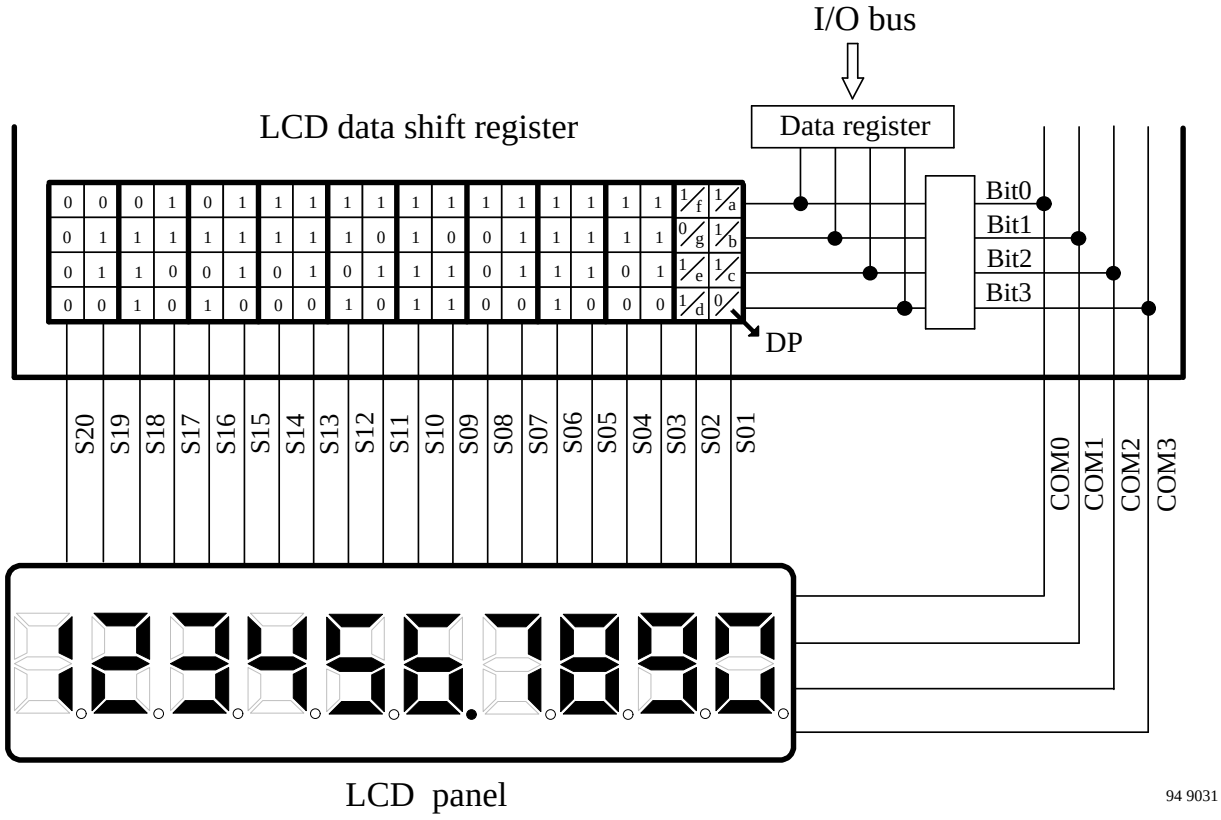
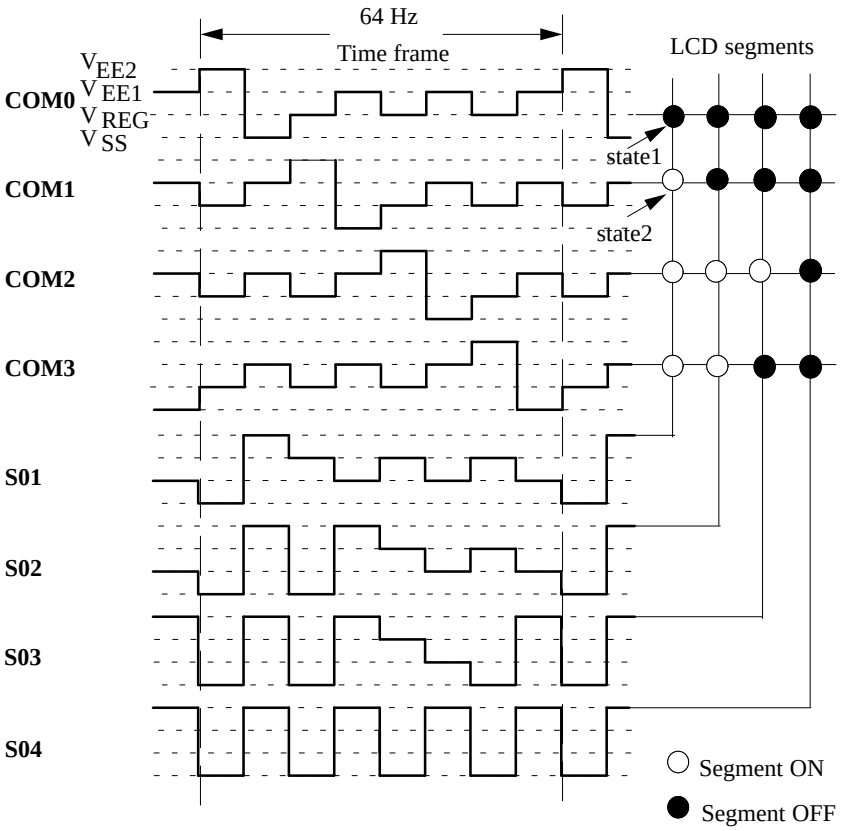
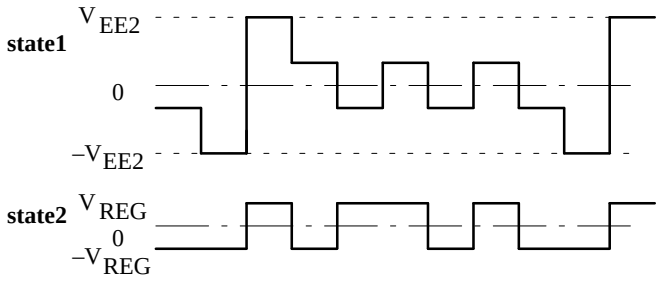


Figure 42. 4:1 multiplex LCD panel connection

(a) Waveforms at driver



(b) Resultant waveforms at LCD segment



94 9032

Figure 43. Waveforms for 4:1 multiplex drive mode

The following formulas are valid in the 4:1 multiplex drive mode at any instant (t):

$V_{State1}(t) = V_{S01}(t) - V_{COM0}(t)$ and $V_{State2}(t) = V_{S02}(t) - V_{COM1}(t)$

$V_{ON(rms)} = \frac{V_{EE2}}{3}\sqrt{3} = 0.577\ V_{EE2}$ and $V_{OFF(rms)} = \frac{V_{EE2}}{3}$

Contrast ratio $= V_{ON(rms)} / V_{OFF(rms)} = 1.732$

5 Electrical Specification

5.1 Absolute Maximum Ratings

All voltages are given relative to $\mathbf{V_{SS}}$. The circuit is protected against supply voltage reversal for typically 5 minutes.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to + 4.0	V
Input voltage (on any pin)	V_{IN}	V_{SS}–0.3 ≤ V_{IN} ≤ V_{DD}+0.3	V
Output short circuit duration	t_{short}	indefinite	s
Operating temperature range	T_{AMB}	–20 to +70	°C
Storage temperature range	T_{stg}	–40 to +125	°C
Thermal resistance (PLCC)	R_{thJa}	70	°C/W
Solder temperature, time	T_{solder}	260°C, 10 s (lead section)	

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device. All inputs and outputs on TEMIC Semiconductors circuits are highly protected against electrostatic discharges. However, precautions to minimize build–up of electrostatic charges during handling are recommended.

For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. $\mathbf{V_{DD}}$).

5.2 DC Operating Characteristics, V_{DD} = 1.5 V, T_{AMB} = +25°C

Supply voltage V_{DD} = 1.5 V, V_{SS} = 0 V, T_{AMB} = +25°C unless otherwise specified.

All voltage levels are measured with reference to $\mathbf{V_{SS}}$ and current flowing into the device is positive.

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Supply voltage		V_{DD}	1.2	1.5	2.4	V
Active current	Note 1	I_{DD}		370	500	µA
Sleep current	Note 2	I_{SLE}		0.9	1.5	µA
Power save current	Note 3, 8	I_{PS}		0.4	0.7	µA
Stop current	Note 8	I_{STOP}			0.1	µA
Supply current quotient	Note 7	$\frac{\lvert I_{DD}\rvert}{f_{RC}}$		0.3	0.4	$\frac{\mu A}{kHz}$
RC oscillator frequency	V_{DD} = 1.5 V; Note 5, 8	f_{RC}	800	1060		kHz
	V_{DD} = 1.2 V		480	580		kHz
Output pads						
Hi-Z leakage current	open drain	I_{OZ}			±20	nA
Output capacitance	Note 8	C_{OUT}		5	10	pF
Input pads (except NRST and OSCIN under test conditions)						
Input voltage high		V_{IH}	0.8*V_{DD}		V_{DD}	V
Input voltage low		V_{IL}	V_{SS}		0.2*V_{DD}	V
Input leakage current (without pull-up or pull-down resistor)	V_{IN} = V_{SS} or V_{IN} = V_{DD}	I_{IN}			± 20	nA
Input capacitance	Note 8	C_{IN}		5	10	pF
NRST and OSCIN input pads under test conditions						
Input voltage high		V_{IH}	V_{DD}		V_{DD}	V
Input voltage low		V_{IL}	V_{SS}		V_{SS}	V

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Bidirectional ports BP00 ... BP03, BP10 ... BP13 and OD						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–0.15	–0.23	–0.45	µA
Output current high	V_{OH} = 1.2 V	I_{OH}	–0.5	–0.6	–0.8	mA
Output current low	V_{OL} = 0.3 V	I_{OL}	0.5	0.7	0.9	mA
Bidirectional port, high current outputs BP40 ... BP41						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–0.15	–0.23	–0.45	µA
Output current high	V_{OH} = 1.2 V	I_{OH}	–1.0	–1.4	–1.8	mA
Output current low	V_{OL} = 0.3 V	I_{OL}	1.4	1.8	2.2	mA
Bidirectional ports BP42 and BP43						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–0.15	–0.23	–0.45	µA
Input current high	$V_{IN} = V_{DD;}$ BP43 only	I_{IH}		5	8	µA
Output current high	V_{OH} = 1.2 V	I_{OH}	–0.5	–0.6	–0.8	mA
Output current low	V_{OL} = 0.3 V	I_{OL}	0.5	0.7	0.9	mA
Bidirectional timer I/O TIM1						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–2	–3.5	–5	µA
Input current high	$V_{IN} = V_{DD}$	I_{IH}		5	8	µA
Output current high	V_{OH} = 1.2 V	I_{OH}	–0.5	–0.6	–0.8	mA
Output current low	V_{OL} = 0.3 V	I_{OL}	0.5	0.7	0.9	mA
Buzzer output INT2						
Output current high	V_{OH} = 1.2 V	I_{OH}	–0.5	–0.6	–0.8	mA
Output current low	V_{OL} = 0.3 V	I_{OL}	0.5	0.7	0.9	mA
Input port IP50 ... IP53						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–2	–3.5	–5	µA
Input current high	$V_{IN} = V_{DD}$	I_{IH}		5	8	µA
Interrupt inputs INT2 and INT7						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–2	–3.5	–6	µA
Input current high	$V_{IN} = V_{DD}$	I_{IH}		5	8	µA
Watchdog WD_EN input						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–3	–4.5	–8	µA
Input current high	$V_{IN} = V_{DD}$	I_{IH}		5	10	µA
NRST input						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–1	–2	–5	µA
Schmitt-trigger input pads INT2, INT7, T1, BP40 and BP41						
Negative going threshold voltage	Note 8	VT–		0.7		V

I_{IL} values are only valid if the pull-up resistor is optioned in

I_{IH} values are only valid if the pull-down resistor is optioned in

5.3 DC Operating Characteristics, V_{DD} = 3 V, T_{AMB} = +25°C

Supply voltage V_{DD} = 3 V, V_{SS} = 0 V, T_{AMB} = +25°C, unless otherwise specified. M44C636 with internal voltage regulator option only.

All voltage levels are measured with reference to V_{SS} and current flowing into the device is positive. Typical parameters represent the statistical mean values.

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Supply voltage		V_{DD}	1.8	3.0	3.6	V
Core supply	$V_{DD} \geq$ 2.2 V; Note 8	V_{INT}	0.9	1.2		V
Active current	Note 1	I_{DD}		100	200	µA
Sleep current	Note 2	I_{SLE}		0.9	1.5	µA
Power save current	Note 3,8	I_{PS}		0.4	0.7	µA
Supply current quotient	Note 7	$\frac{\lvert I_{DD}\rvert}{f_{RC}}$		0.3	0.4	$\frac{\mu A}{kHz}$
RC oscillator frequency	V_{INT} = 1.2 V	f_{RC}	400	560		kHz
Output pads						
Hi-Z leakage current	Open drain	I_{OZ}			±20	nA
Output capacitance	Note 8	C_{OUT}		5	10	pF
Input pads (except NRST and OSCIN under test conditions)						
Input voltage high		V_{IH}	0.8^{*} V_{DD}		V_{DD}	V
Input voltage low		V_{IL}	V_{SS}		$0.2*V_{DD}$	V
Input leakage current (without pull-up or pull-down resistor)	$V_{IN} = V_{SS}$ or $V_{IN} = V_{DD}$	I_{IN}			±20	nA
Input capacitance	Note 8	C_{IN}		5	10	pF
NRST and OSCIN input pads under test conditions						
Input voltage high		V_{IH}	V_{DD}		V_{DD}	V
Input voltage low		V_{IL}	V_{SS}		V_{SS}	V

Bidirectional ports BP00 ... BP03, BP10 ... BP13 and OD						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–1.0	–1.3	–2.0	µA
Output current high	V_{OH} = 2.4 V	I_{OH}	–1.7	–2.2	–2.7	mA
Output current low	V_{OL} = 0.6 V	I_{OL}	2.0	2.5	3.0	mA
Bidirectional ports high BP40 ... BP41 (watch motor drive capability)						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–1.0	–1.3	–2	µA
Output voltage high	I_{OH} = –1 mA	$V_{DD}–V_{OH}$	100	160	200	mV
Output voltage low	I_{OL} = 1 mA	V_{OL}	50	130	150	mV
Output voltage high	I_{OH} = –1 mA V_{DD} = 2.2 V	$V_{DD}–V_{OH}$	100	180	225	mV
Output voltage low	I_{OL} = 1 mA V_{DD} = 2.2 V	V_{OL}	50	150	175	mV
Output current high	V_{OH} = 2.7 V; Note 8	I_{OH}	–1.4	–1.9	–2.5	mA
Output current low	V_{OL} = 0.3 V; Note 8	I_{OL}	1.7	2.3	2.8	mA
Bidirectional ports BP42 and BP43						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–1.0	–1.3	–2.0	µA
Input current high	$V_{IN} = V_{DD;}$ BP43 only	I_{IH}	25	35	45	µA
Output current high	V_{OH} = 2.4 V	I_{OH}	–1.7	–2.2	–2.7	mA
Output current low	V_{OL} = 0.6 V	I_{OL}	2.0	2.5	3.0	mA

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Bidirectional timer I/O TIM1						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–15	–21	–30	µA
Input current high	$V_{IN} = V_{DD}$	I_{IH}	25	34	45	µA
Output current high	V_{OH} = 2.4 V	I_{OH}	–1.7	–2.2	–2.7	mA
Output current low	V_{OL} = 0.6 V	I_{OL}	2.0	2.5	3.0	mA
Buzzer output INT2						
Output current high	V_{OH} = 2.4 V	I_{OH}	–1.7	–2.2	–2.7	mA
Output current low	V_{OL} = 0.6 V	I_{OL}	2.0	2.5	3.0	mA
Input ports IP50 ... IP53 and WD_EN						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–20	–28	–40	µA
Input current high	$V_{IN} = V_{DD}$	I_{IH}	25	35	45	µA
Interrupt inputs INT2 and INT7						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–30	–40	–50	µA
Input current high	$V_{IN} = V_{DD}$	I_{IH}	40	49	60	µA
NRST input						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–7	–12	–20	µA
Schmitt-trigger input INT2, INT7, TIM1, BP40 and BP41						
Negative going threshold voltage	Note 8	VT–		1.6		V

I_{IL} values are only valid if the pull-up resistor is optioned in

I_{IH} values are only valid if the pull-down resistor is optioned in

5.4 DC Operating Characteristics, V_{DD} = 1.2 to 3.6 V, T_{AMB} = +25°C

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
LCD driver (3 V LCD panel)	**Segment outputs: S01 ... S20** **Backplane outputs: COM0 ... COM3**					
Regulated voltage	Note 6	V_{REG}	0.9	1.0	1.1	V
Doubler voltage	V_{REG} = 1.0 V	V_{EE1}	1.75	2.0	2.1	V
Triple voltage	V_{REG} = 1.0 V	V_{EE2}	2.7	3.0		V
Temperature compensation	relative to V_{REG}; Note 8	T_{REG}	–5	–5.5	–6	$\frac{mV}{°C}$
Backplane frequency	4:1 multiplex	f_{BP}		64		Hz
	3:1 multiplex			43		Hz
	2:1 multiplex			64		Hz
	Direct drive			128		Hz
Segment output resistance	ΔV_{SEG} = 100 mV; Note 8	R_{SO}		4.5	6	kΩ
Backplane output resistance	ΔV_{BP} = 100 mV; Note 8	R_{BO}		2.2	3	kΩ
Average DC offset voltage	Note 8	V_{DC}		10	50	mV
Quarz oscillator						
Frequency	C_L = 10 pF	f_C		32,768		Hz
Integrated input capacitance	Note 8	C_{OSCIN}	15	20		pF
Integrated output capacitance	Note 8	C_{OSCOUT}	15	20		pF
Stability	ΔAV_{DD} = 100 mV; Note 8	Δf/f		0.1	1.0	ppm
Start up time	AV_{DD} = 1.4 V	t_{SQ}		1	2	s

Note 1: Maximum active current (I_{DD})

This is the current observed at the V_{SS} pin with the crystal oscillator, the LCD driver and µC core permanently active. No output loads, all input ports and interrupt inputs connected to V_{DD} and the prescaler is reset. This mode can be achieved by connecting the **NRST** pin to V_{SS}. The average system current of an application can be estimated with the formula:

I_{SYS}:= I_{SLE} + (duty cycle / 100% x I_{DD}), whereby Duty cycle:= active time x 100%/(sleep time + active time)
I_{DD}:= 200 µA; I_{SLE} = 1 µA at 1.5 V

In timekeeping mode the duty cycle is typically less than 1%, which gives a current consumption of less than 3 µA at 1.5 V.

Note 2: Sleep current (I_{SLE})

This is the current taken with the crystal oscillator and the LCD driver active, the prescaler reset, and µC core in SLEEP mode and all input ports, bidirectional ports (if in input mode) and interrupts connected to V_{DD}. This state can only be permanently achieved at the end of the stimulated selftest program.

Note 3: Power save current (I_{PS})

This is the current taken with the crystal oscillator active, the prescaler reset, the µC core in SLEEP mode, the LCD driver in the power saving mode and all input ports, bidirectional ports (if in input mode) and interrupts connected to V_{DD}. This state can, unless used in the application program, only be permanently achieved under production test conditions.

Note 4: Power-on reset voltage (V_{POR})

This is the supply voltage, which must be exceeded for the internal power-on reset circuit to be released. For a proper operation of the CPU during power-up and at supply voltages below 1.8 V an external capacitor of 470 nF to 2.2 µF has to be connected between **NRST** and V_{SS}. This capacitor may be omitted only when a linear power supply voltage rise

of $\frac{dV}{dt} \geq \frac{50\ mV}{msec}$ can be guaranteed in the application.

Note 5: RC oscillator frequency (F_{RC})

The RC oscillator provides the central clocking of the frequency varies with supply voltage and temperature to track the optimum performance of the µC. This frequency can be measured on the **TCL** pin by connecting the **NRST and TST1** pins to V_{SS} before power on reset.

Note 6: LCD voltages are measured with

– 100 nF capacitor between **C1** and **C2**
– 100 nF capacitor between V_{EE1} and V_{SS}
– 100 nF capacitor between V_{EE2} and V_{SS}

A load capacitance of 200 pF is connected between each backplane and V_{SS}. The regulated and temperature compensated LCD voltage V_{REG} can also be supplied from an external voltage source through the V_{REG} pin, as long as the externally supplied voltage is larger than the internally generated voltage. It is also possible to supply all three LCD voltage levels through the pads V_{REG}, V_{EE1} and V_{EE2} as it is done under production test conditions.

Note 7: Supply current quotient

Normalized active current relative to the core's operation frequency. The frequency of the integrated RC oscillator depends on the supply voltage as well as on the process parameters (i.e. sum of threshold voltages).

Note 8: Measurement not subject to production test

Table 17. Standard crystal specification

Parameter	Symbol	Typ.	Max.	Unit
Frequency	f	32,768	40,000	Hz
Series resistance	R_S	30	50	kΩ
Static/shunt capacitance	C_0	1.5		pF
Dynamic capacitance	C_1	3		fF
Load capacitance	C_L	10	12.5	pF

6 Mechanical Data

This chapter contains the pad layout and pad coordinates. The pin-out for packaged parts in QFP64 and PLCC44 is shown too. The 64 pin ceramic DIL package which is used for emulation and prototype evaluation purposes is included.

6.1 Emulation Packages

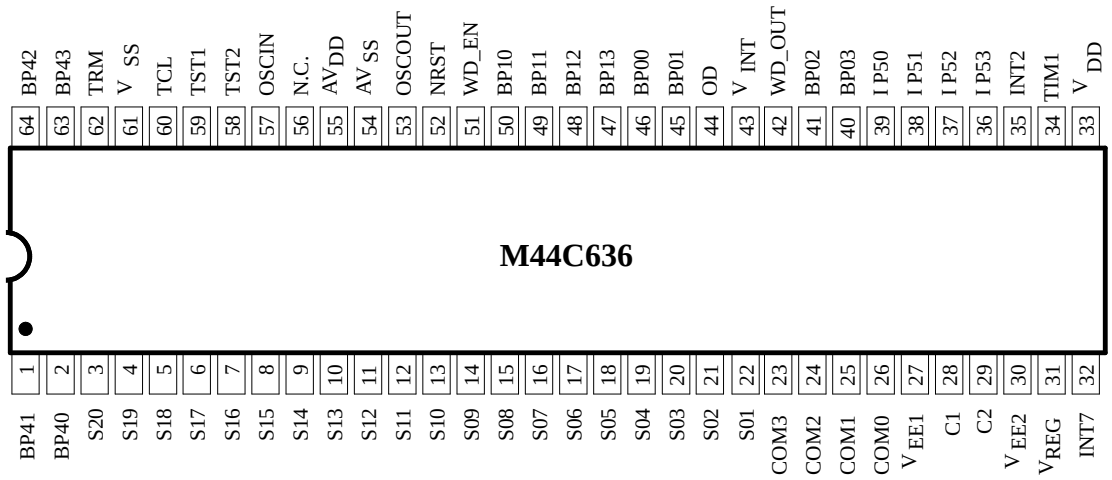


Figure 44. Emulation package – 64 pin ceramic DIL

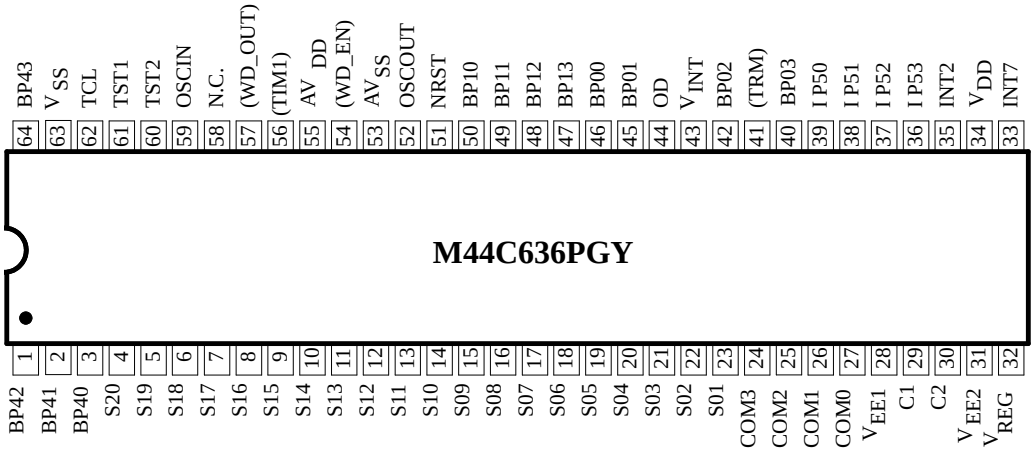


Figure 45. Pin-out of M44C636 piggyback and target board adapter

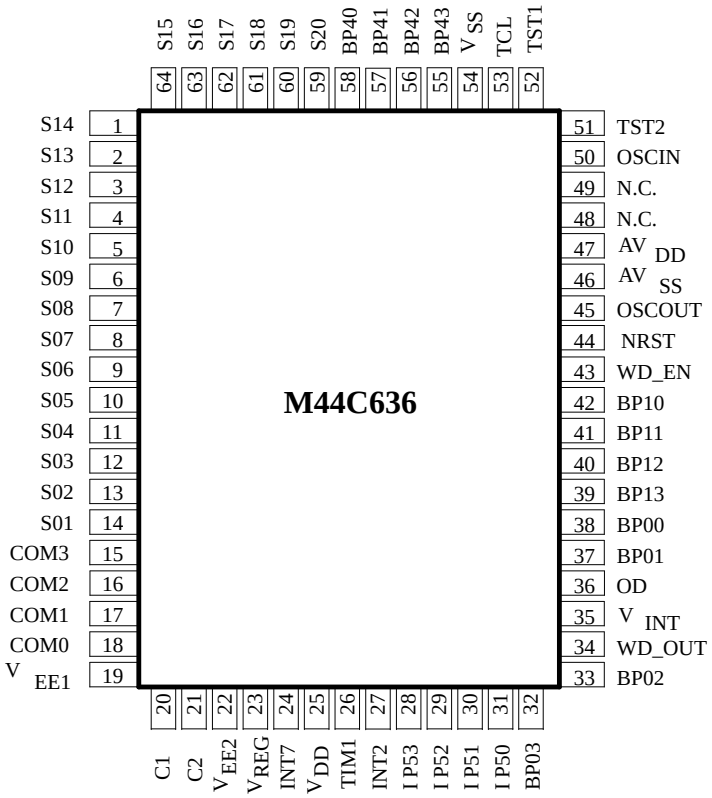


Figure 46. M44C636 in 64 pin plastic QFP (top view)

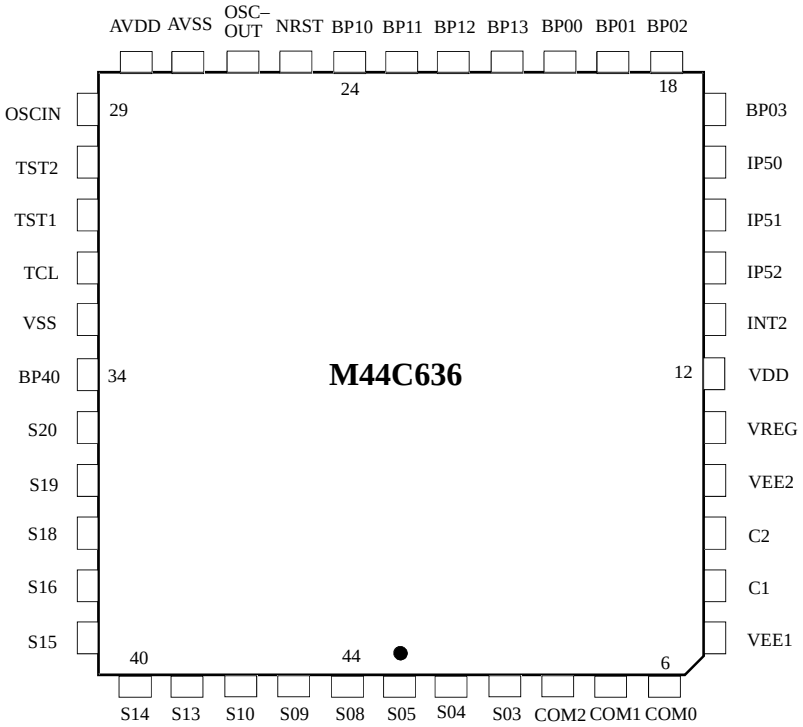


Figure 47. M44C636 in 44 pin PLCC (top view)

6.2 Pad Layout

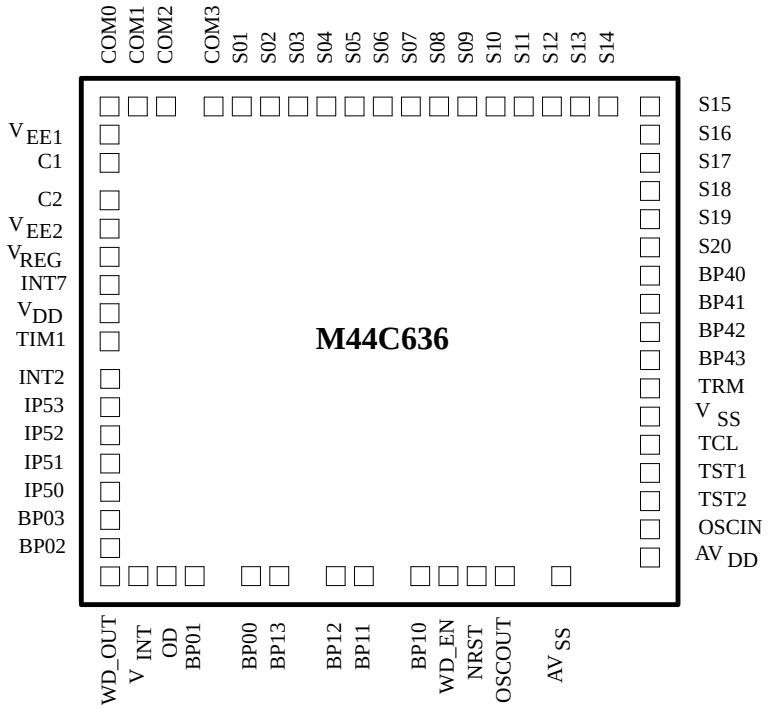


Figure 48. M44C636 pad configuration

6.3 Pad Coordinates

The M44C636 is also available in die form for COB mounting. Therefore the substrate, i.e. the backside of the die, should be connected to $\mathbf{V_{SS}}$.

Die size: 3.874 x 3.514 mm = 13.61 mm^2
Pad size: 100 x 100 µm
Thickness: 400 ± 25 µm

Table 18. Pad coordinates of M44C636

No.	Name	X Point	Y Point
1	NST	0	0
2	V_{INT}	217.6	0
3	OD	463.6	18
4	BP01	639.6	18
5	BP00	943.6	18
6	BP13	1,119.6	18
7	BP12	1,423.6	18
8	BP11	1,599.6	18
9	BP10	1,903.6	18
10	WD_EN	2,079.6	18
11	NRST	2,245.6	18
12	OSCOUT	2,422.6	18
13	AV_{SS}	2,694.2	18
14	AV_{DD}	3,500.4	–39.8
15	OSCIN	3,500.4	127.2
16	TST2	3,500.4	303.2
17	TST1	3,500.4	469.2
18	TCL	3,500.4	645.2
19	V_{SS}	3,500.4	879.0
20	TRM	3,500.4	1,055.0
21	BP43	3,500.4	1,231.0
22	BP42	3,500.4	1,535.0
23	BP41	3,500.4	1,711.0
24	BP40	3,500.4	2,127.0
25	S20	3,500.4	2,346.2
26	S19	3,500.4	2,512.2
27	S18	3,500.4	2,688.2
28	S17	3,500.4	2,854.2
29	S16	3,500.4	3,030.2
30	S15	3,500.4	3,196.2
31	S14	3,213.2	3,152.4
32	S13	3,037.2	3,152.4
33	S12	2,871.2	3,152.4
34	S11	2,695.2	3,152.4
35	S10	2,529.2	3,152.4
36	S09	2,353.2	3,152.4
37	S08	2,187.2	3,152.4
38	S07	2,011.2	3,152.4
39	S06	1,845.2	3,152.4
40	S05	1,669.2	3,152.4
41	S04	1,503.2	3,152.4
42	S03	1,327.2	3,152.4
43	S02	1,161.2	3,152.4
44	S01	985.2	3,152.4
45	COM3	819.2	3,152.4
46	COM2	396.8	3,152.4
47	COM1	230.8	3,152.4
48	COM0	0	3,196.2
49	V_{EE1}	0	3,030.2
50	C1	0	2,854.2
51	C2	0	2,526
52	V_{EE2}	0	2,350
53	V_{REG}	0	2,162
54	INT7	0	1,996
55	V_{DD}	0	1,820
56	TIM1	0	1,644
57	INT2	0	1,340
58	IP53	0	1,164
59	IP52	0	998
60	IP51	0	822
61	IP50	0	656
62	BP03	0	480
63	BP02	0	176

7 M44C636 – Timer Application

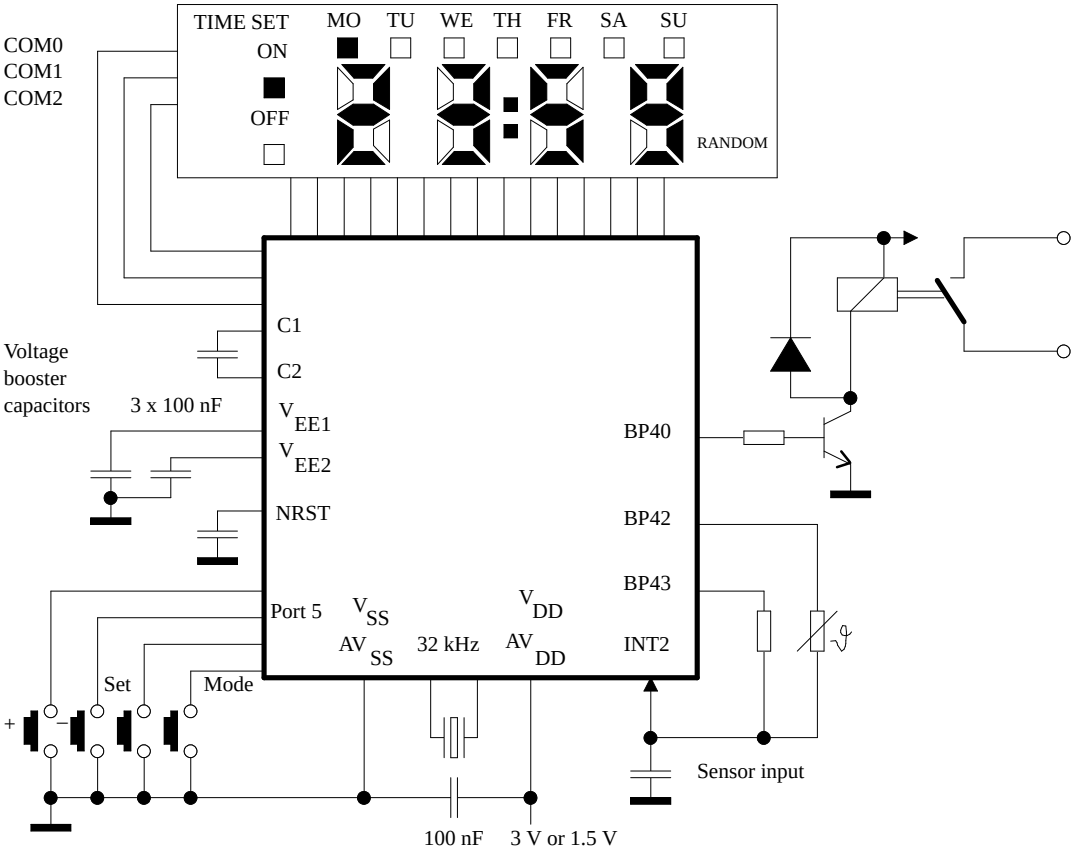


Figure 49. Application example

8 Ordering Information

Please insert ROM CRC and select the option setting from the list below.

BP40
- ❑ CMOS
- ❑ Open drain [N]
- ❑ Open drain [P]
- ❑ Pull-up

BP41
- ❑ CMOS
- ❑ Open drain [N]
- ❑ Open drain [P]
- ❑ Pull-up

MOT driver
- ❑ 1 kHz chopping frequency
- ❑ 2 kHz chopping frequency

Duty: ❑ $^3/_8$ ❑ $^1/_2$ ❑ $^5/_8$ ❑ $^3/_4$

BP42
- ❑ CMOS
- ❑ Open drain [N]
- ❑ Open drain [P]
- ❑ Pull-up

Fout
- ❑ 32 kHz output with 50% duty
- ❑ 8 kHz output with 50% duty
- ❑ 8 kHz output with 75% duty

BP43
- ❑ CMOS
- ❑ Open drain [N]
- ❑ Open drain [P]
- ❑ Pull-up
- ❑ Pull-down

IP50
- ❑ Pull-up
- ❑ Pull-down

IP51
- ❑ Pull-up
- ❑ Pull-down

IP52
- ❑ Pull-up
- ❑ Pull-down

IP53
- ❑ Pull-up
- ❑ Pull-down

IP5 INT
- ❑ Negative edge triggered
- ❑ Positive edge triggered
- ❑ Interrupt priority 1 (default)
- ❑ Interrupt priority 4

Coded reset
- ❑ Not used
- ❑ RST2 (IP50 & IP51)
- ❑ RST3 (IP50 & IP51 & IP52)
- ❑ RST4 (IP50 ... IP53)

Watchdog
- ❑ Hardware disabled
- ❑ Software enabled (WD_EN: Pull-up)
- ❑ HW enabled (WD_EN: pull down)

- ❑ $^1/_2$ Hz
- ❑ 1 Hz
- ❑ 2 Hz

TIM1
- ❑ CMOS
- ❑ Open drain [N]
- ❑ Open drain [P]
- ❑ Pull-up

Buzzer
- ❑ CMOS
- ❑ Open drain [N]
- ❑ Open drain [P]

INT2
- ❑ Pull-up
- ❑ Pull-down

INT7
- ❑ Pull-up
- ❑ Pull-down

OSCIN
- ❑ No integrated capacitance
- ❑ Internal CAP (_ pF)

OSCOUT
- ❑ No intergrated capacitance
- ❑ Internal CAP (_ pF)

Core supply
- ❑ Internal regulator ($V_{DD} \geq 1.8$ V)
- ❑ $V_{DD} \leq 1.8$ V

Package
- ❑ DIT
- ❑ PLCC44
- ❑ QFP64
- ❑ SSO44

ROM code
- ❑ Stimulus at Port 0: _____ for conditional self tests

File
- ❑ _____.HEX
- ❑ CRC: _____

TYPE: Normal/Short

Approval Date: ___.___.___ Signature: _____

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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